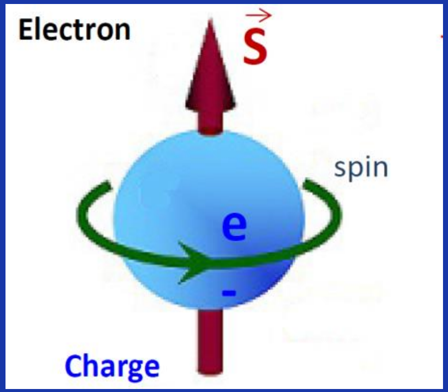
Science et Progrès, 24 mars 2022, présentation d'Albert Fert
prof. à l'Université Paris-Saclay, Umφ CNRS-Thales

Spintronique: électronique sobre en énergie et plus encore
(*spintronics to go beyond electronics and switch greener*)



CNRS THALES université PARIS-SACLAY

Spintronique: électronique sobre en énergie et plus encore (*spintronics to go beyond electronics and switch greener)*

I Dépasser l'électronique classique, pourquoi?

II Rapide introduction à la spintronique

III Composants Spintronique (STT-RAM, SOT-RAM..) pour Technologies de l'Information et Communication plus frugales

IIII Quelques mots sur skyrmions, ordinateurs neuromorphiques etc..

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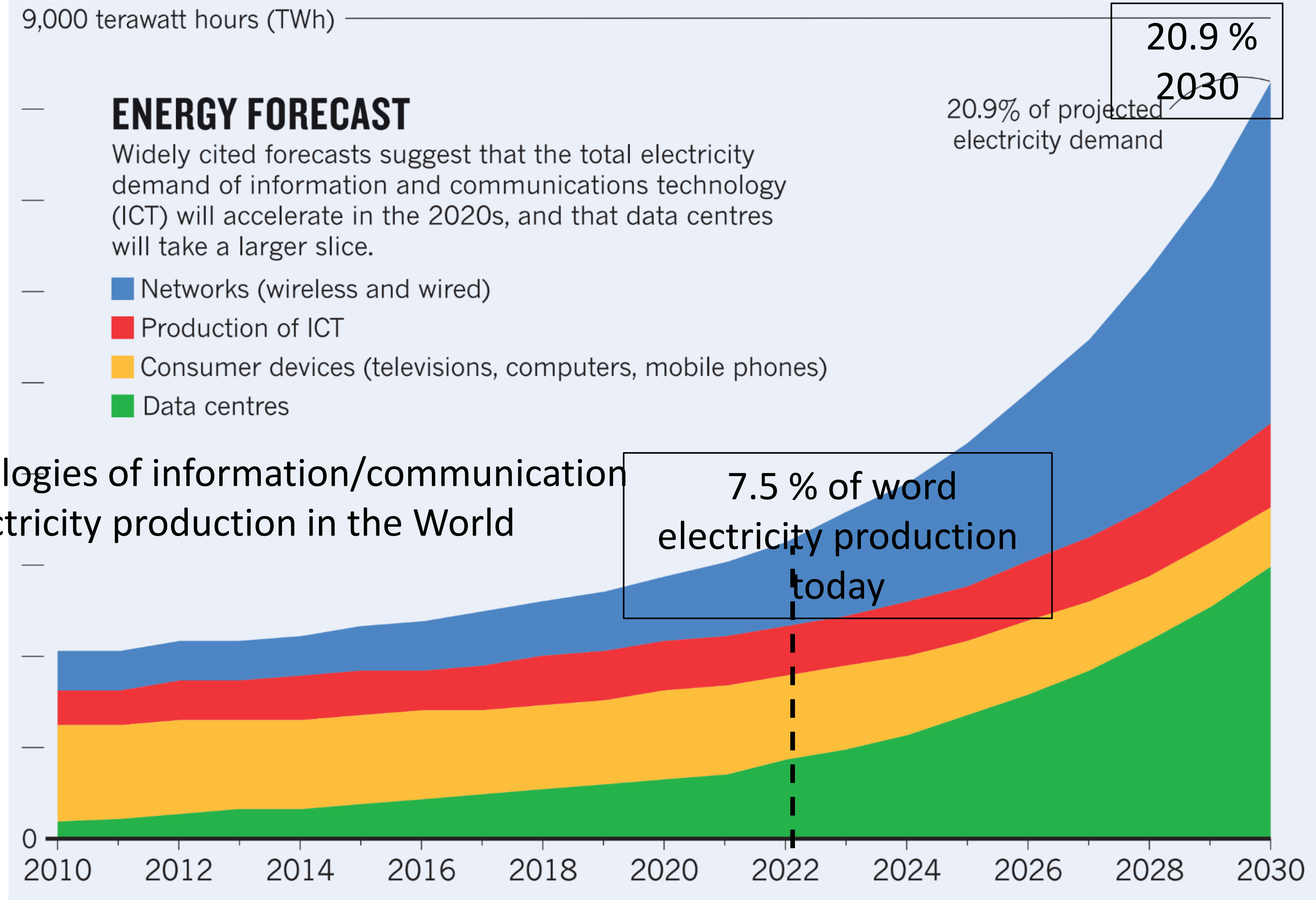
(specific objectives with spintronics)

Low power logic/memory components for our computers, phones (reducing energy consumption of information and communication technologies and their significant contibution to global warming is one of the aims)

Birth of novel technologies: skyrmionics, neuromorphic computers with spintronic nano-components, magnonics



Demand of the technologies of information/communication in % of the electricity production in the World

Andrea and Edler; Challenges, 6, 117 (2015) ; N. Jones, Nature 561, 163 (2018)

5.8 Terawatt hours

San Francisco

5.7 Terawatt hours (2015)

Google

Increase of 30%/year

30 Google searches cost as much energy as to bring a liter of water to boil

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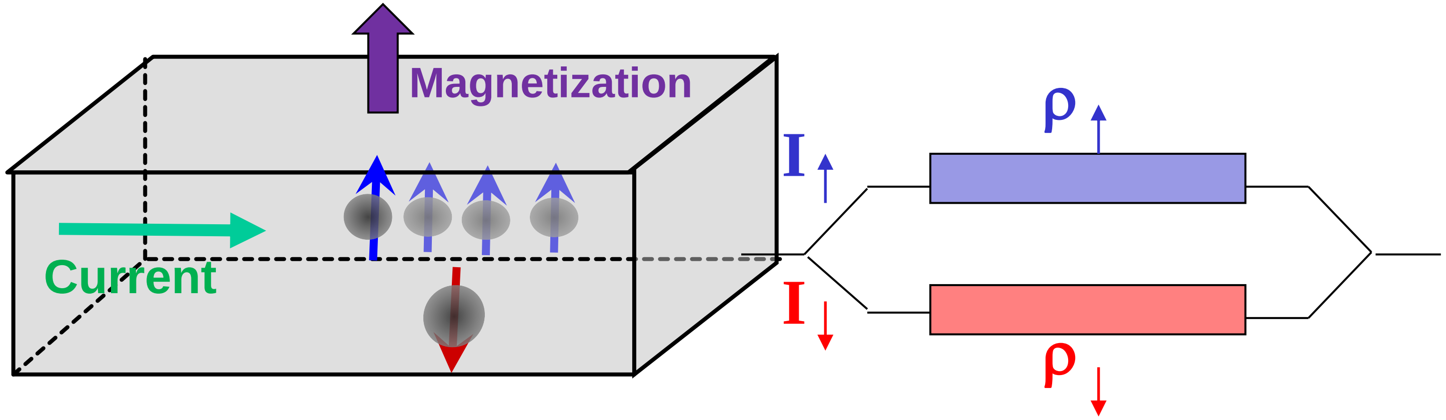
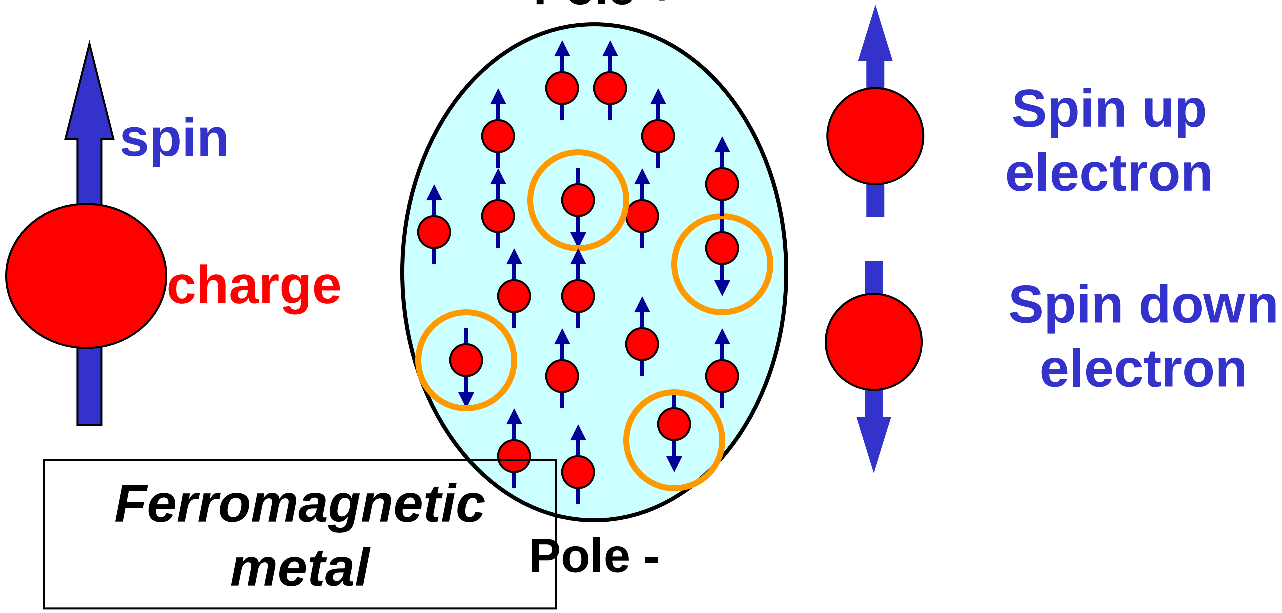
From magnetism to spin dependent conduction, GMR and Spintronics

Spin-polarized current in a ferromagnetic metal





From Ph.D. work to Giant Magnetoresistance (GMR) and Spintronics

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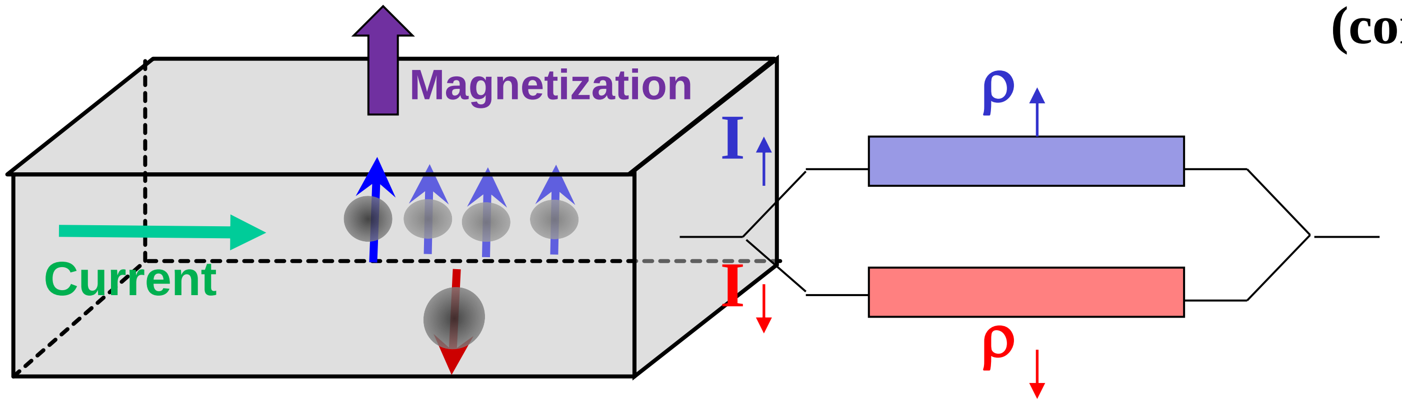
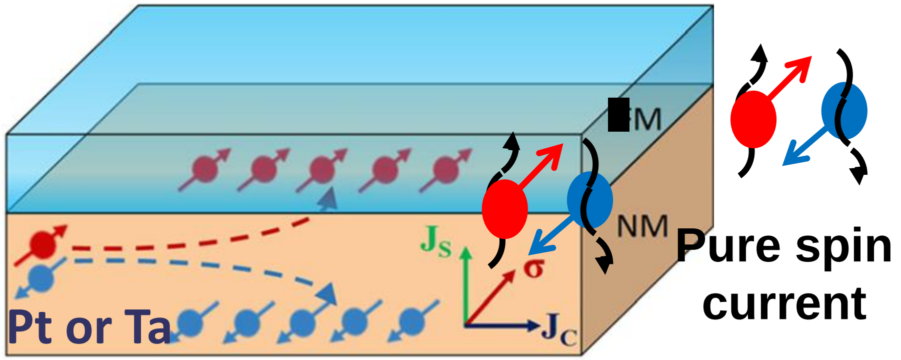
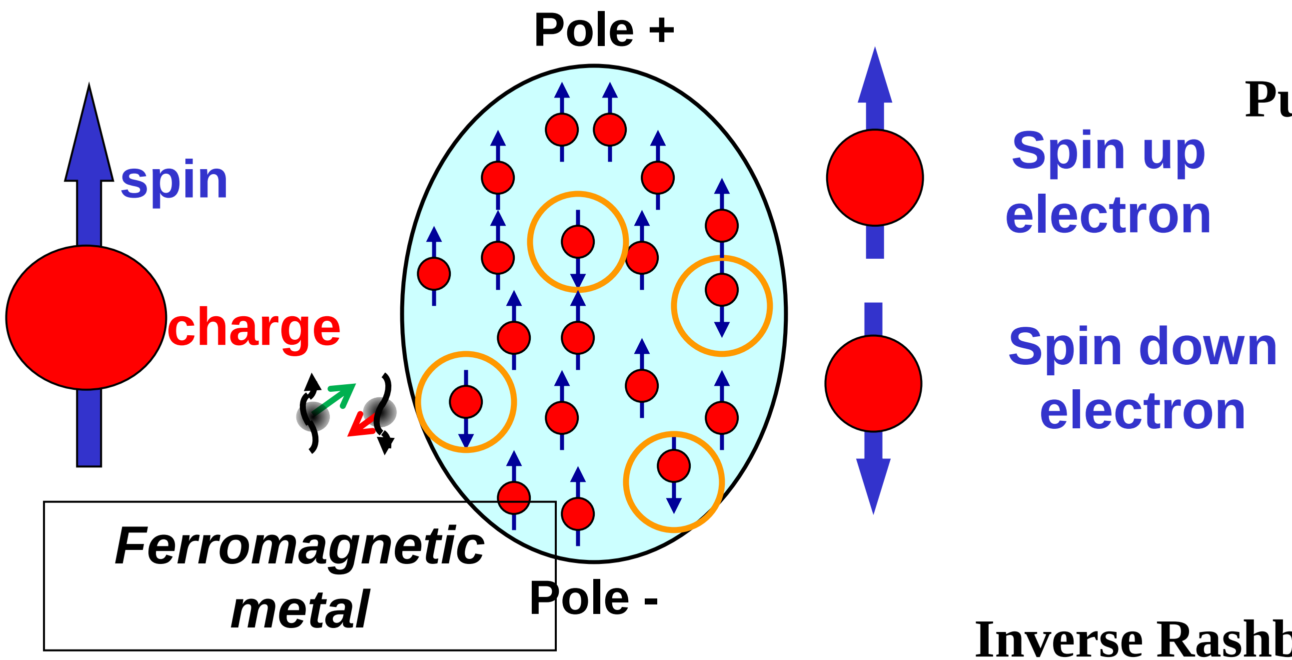


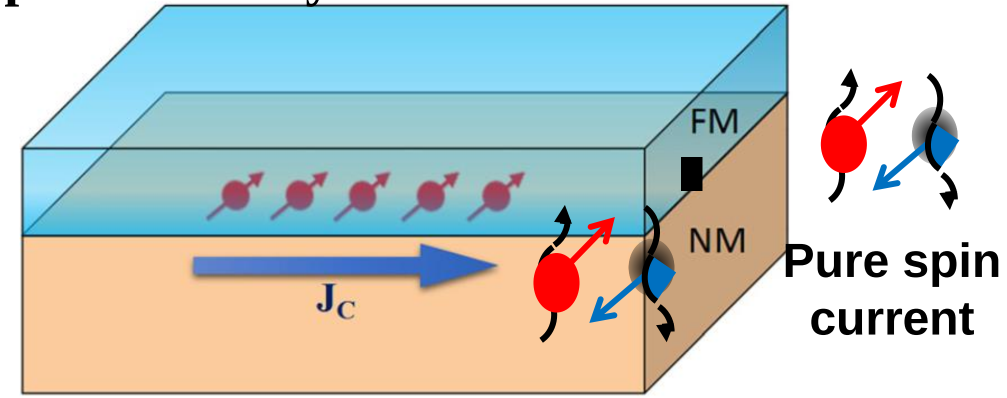
Pure spin current induced by Spin Hall Effect in HM (conversion from charge to spin current)



Spin Hall effect



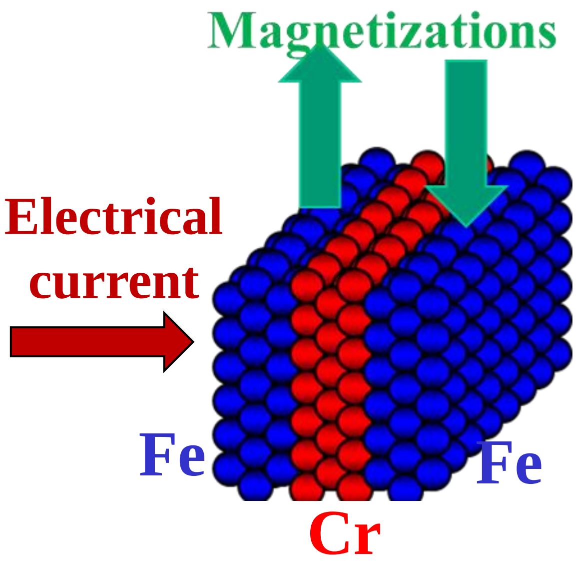
Pure spin current by interfacial Edelstein effect



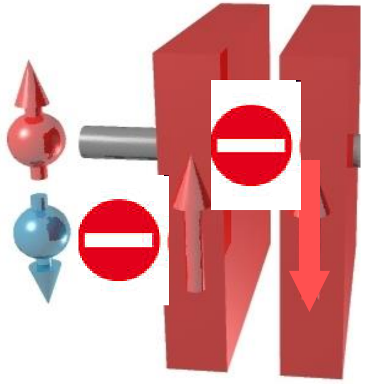
Rashba-Edelstein effect

Inverse Rashba-Edelstein effect: injected spin current generates charge curent (conversion from spin to charge current)

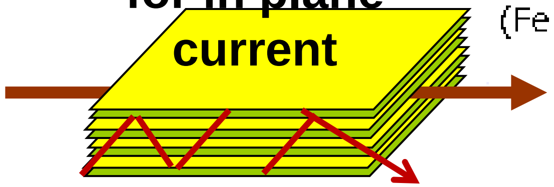
• Giant Magnetoresistance (GMR)
(Orsay, 1988, Fe/Cr multilayers, Jülich, 1989, Fe/Cr/Fe trilayers)

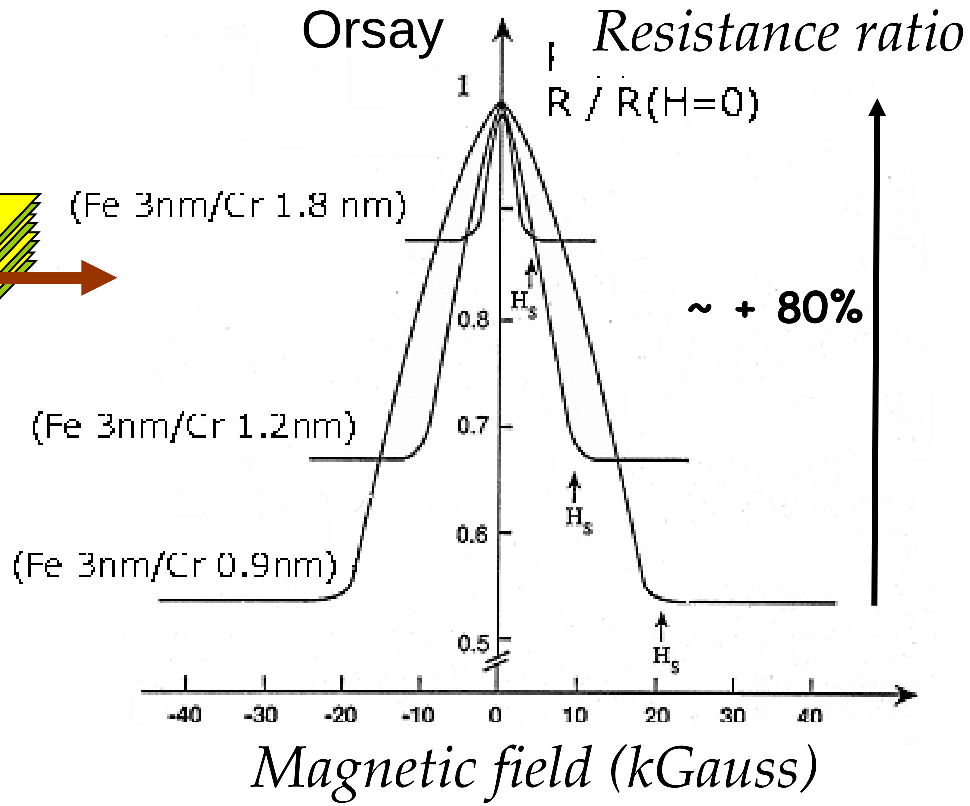


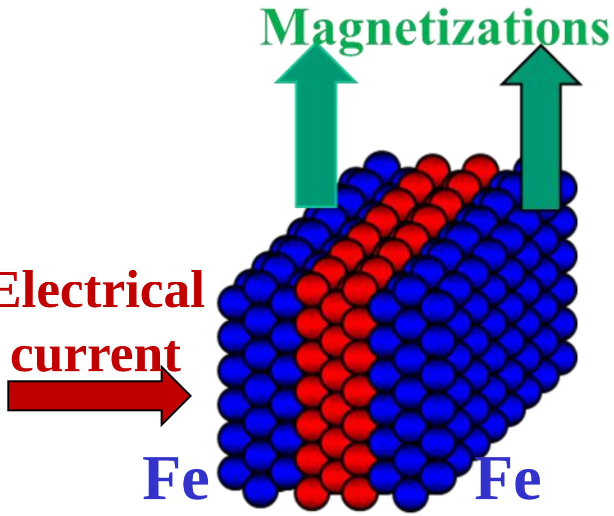
Opposite magnetizations: the current does not flow



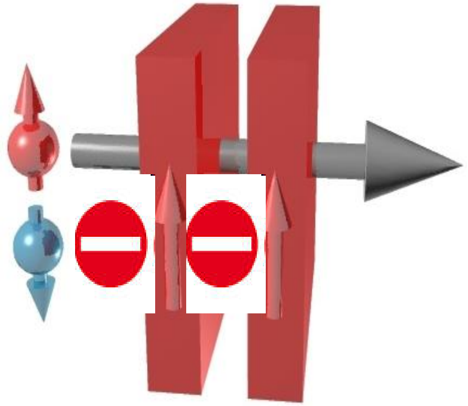
Works also for in plane current

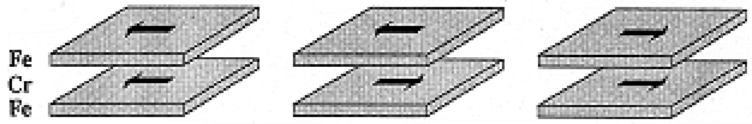






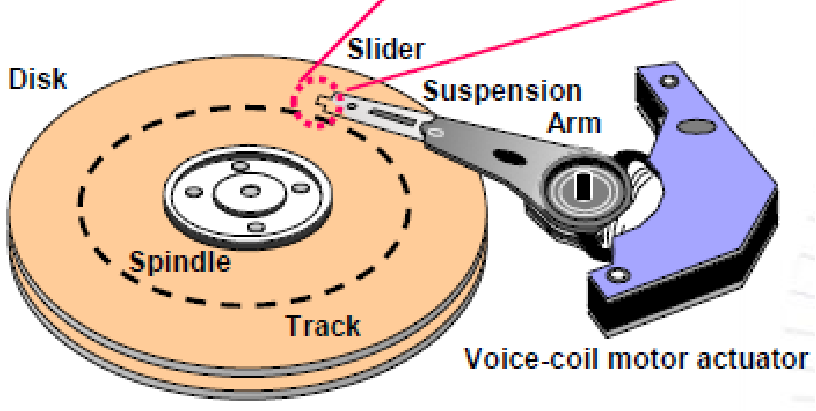
The current flows if a magnetic field aligns the magnetizations

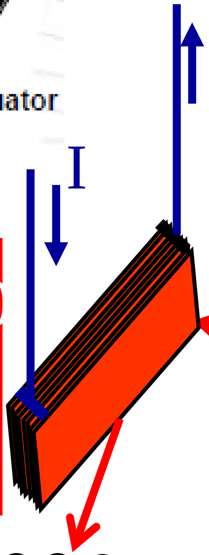


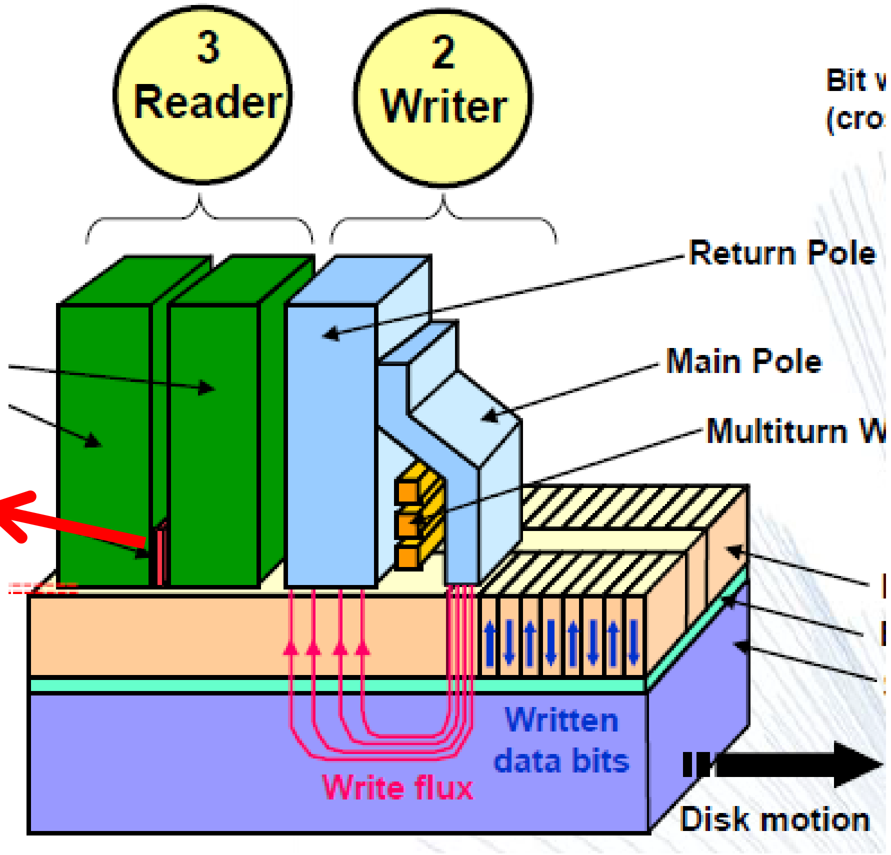


AP (AntiParallel) **P** (Parallel)

Magnetic multilayers, magnetic tunnel junctions in the read heads of hard disks of today and perspective for tomorrow

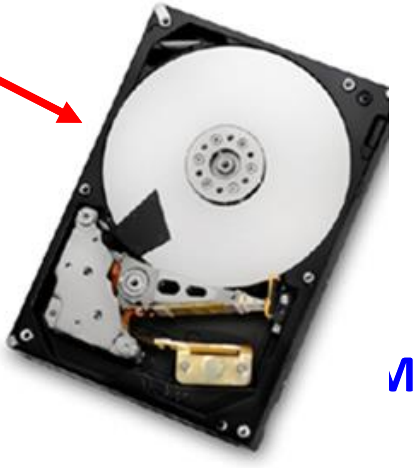


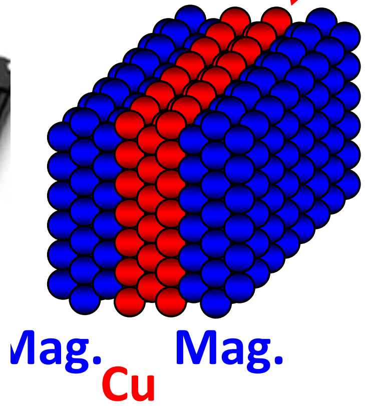




GMR sensor (Magn. Multilayer)
or TMR sensor
(Magn. Tunnel Junction)

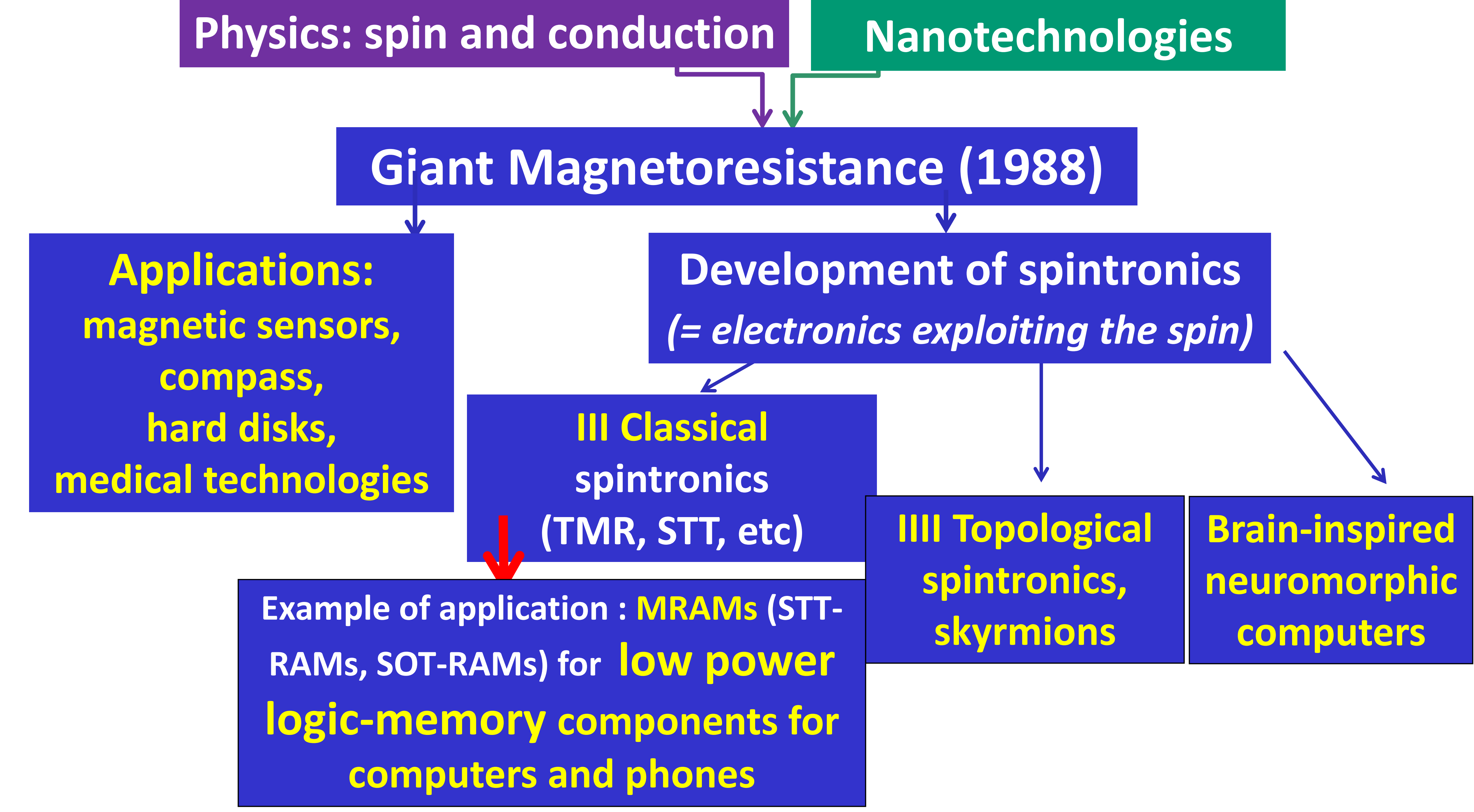
10 Tbyte HDD
(Large capacity HDD, a boost for the development of data centers)





before GMR (< 1997) : 1 Gbit/in^2

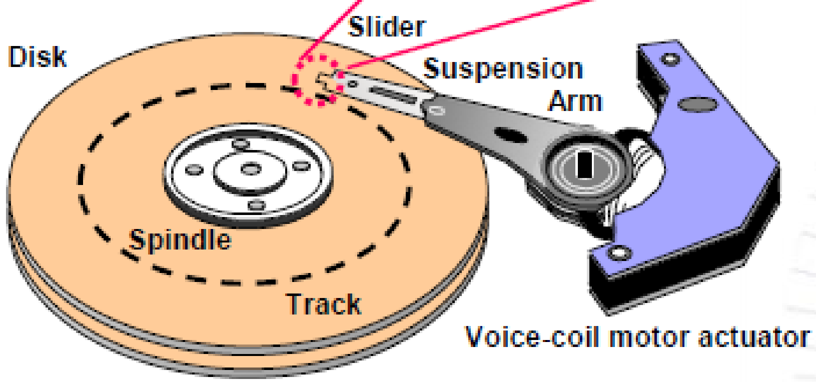
today with GMR (or TMR) : ≈ 1000 Gbit/in^2

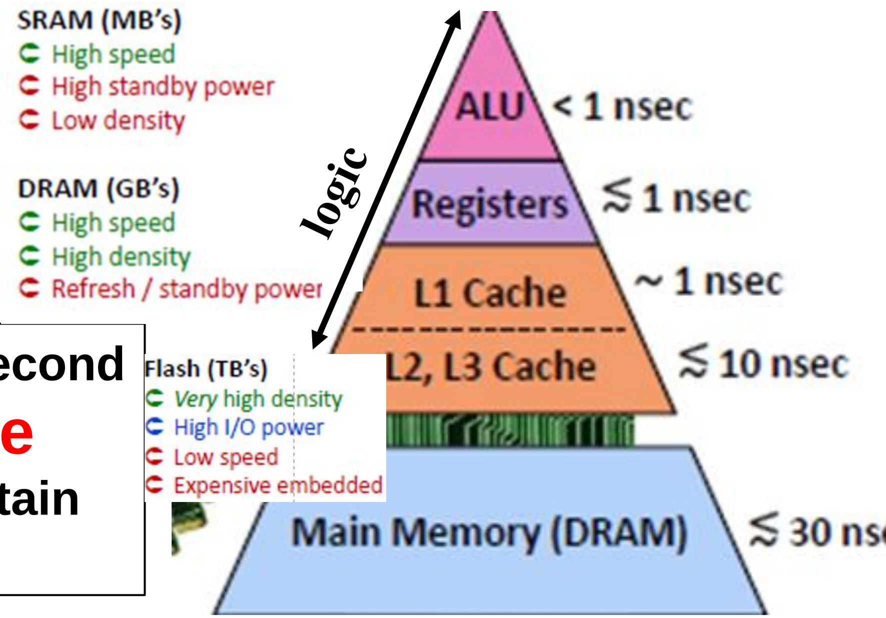

Physics: spin and conduction
Nanotechnologies
Giant Magnetoresistance (1988)
Applications:
magnetic sensors,
compass,
hard disks,
medical technologies
Development of spintronics
(= electronics exploiting the spin)
III Classical
spintronics
(TMR, STT, etc)
IIII Topological
spintronics,
skyrmions
Brain-inspired
neuromorphic
computers
Example of application : MRAMs (STT-RAMs, SOT-RAMs) for low power logic-memory components for computers and phones

RAMs (Randon Access Memories), MRAMs, STT-MRAMs, SOT-MRAMs

Storage: Hard Disk (up to 10Tbyte) or Flash memory (less, expensive)

Inside computer: Logic circuits (logic gates) + RAMs (Random Acess Memory: DRAM, SRAM, standalone or « embedded » in logic circuits), ex: 16 Gb





Massive memory, HDD (and Flash): non-volatile but slow (ms)

RAM: High speed (≈ nanosecond for S-RAM) but volatile (electrical energy to maintain memory alive)

Réduction of energy consumption (« low power ») with non-volatile spintronic MRAMs: Magnetic-RAM (MRAM), today STT-MRAM (on market), tomorrow SOT-MRAM

STT-RAM comes to reality

Example of product:
GT2 Huawei smart watch

TSMC to start eMRAM production in 2018

Jun 08, 2017 **MRAM production**

According to reports, Taiwan Semiconductor Manufacturing Company (TSMC) is aiming to start producing embedded MRAM chips in 2018 using a 22 nm process. This will be initial "risk production" to gauge market reception.

Europe: Global Foundaries is ramping up STT-RAM production in Dresden + Devel. by IMEC

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Samsung ready to mass produce MRAM chips using 28nm FD-SOI process

Yiling Lin, Taipei; Jessie Shen, DIGITIMES [Tuesday 26 September 2017]

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In related news, Synopsys announced recently its Design Platform has been fully certified for use on Samsung Foundry's 28nm FD-SOI process technology. A PDK and a comprehensive reference flow, compatible with Synopsys' Lynx Design System, containing scripts, design methodologies and best practices is now available.

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GF-Everspin 2X nm eMRAM with superior data retention - VLSI Symposium

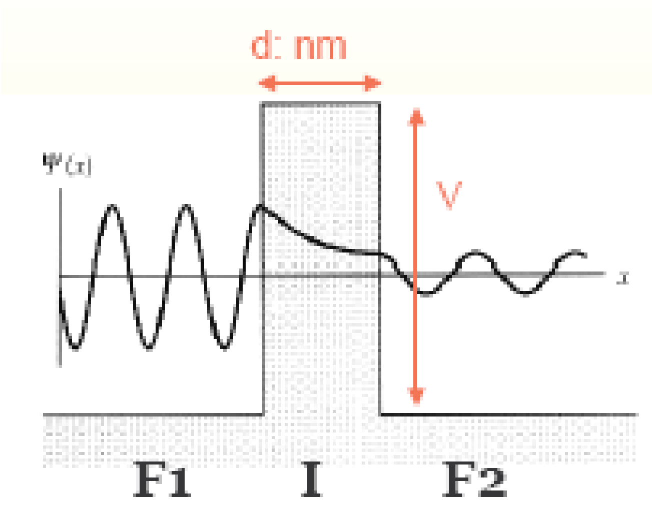
GLOBALFOUNDRIES and Everspin continue to drive embedded MRAM (eMRAM) forward into the 22nm process node! Please see our technical paper presented this week at VLSI Symposium in Japan.

For the first time, we are unveiling eMRAM that can retain data through solder reflow at 260C and 10+ years at 125C, plus read/write with outstanding endurance at 125C.

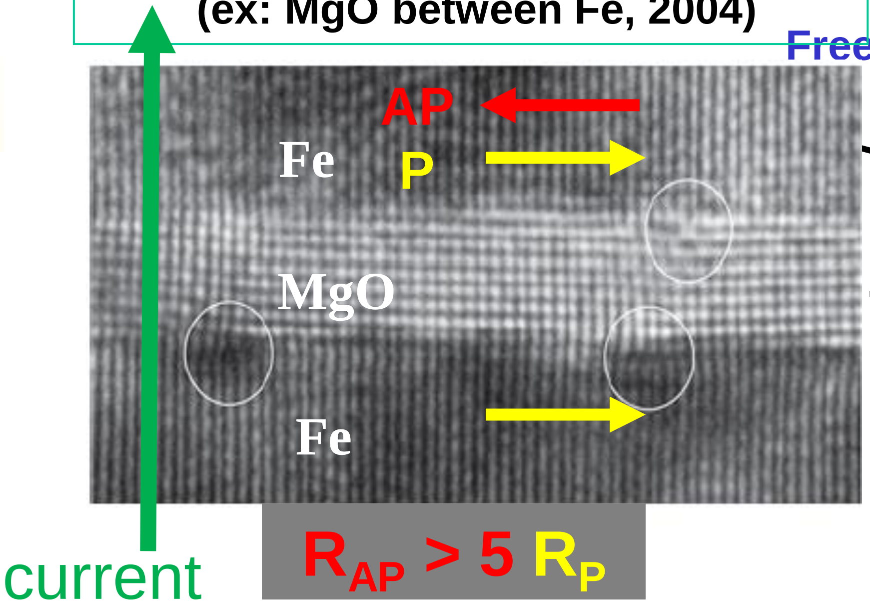
This is a major breakthrough from GLOBALFOUNDRIES and Everspin that enables eMRAM to be used fc general purpose MCU's and Automotive SOCs.

Magnetic Tunnel Junctions, Spin Transfer Torque (STT) ad STT-MRAM

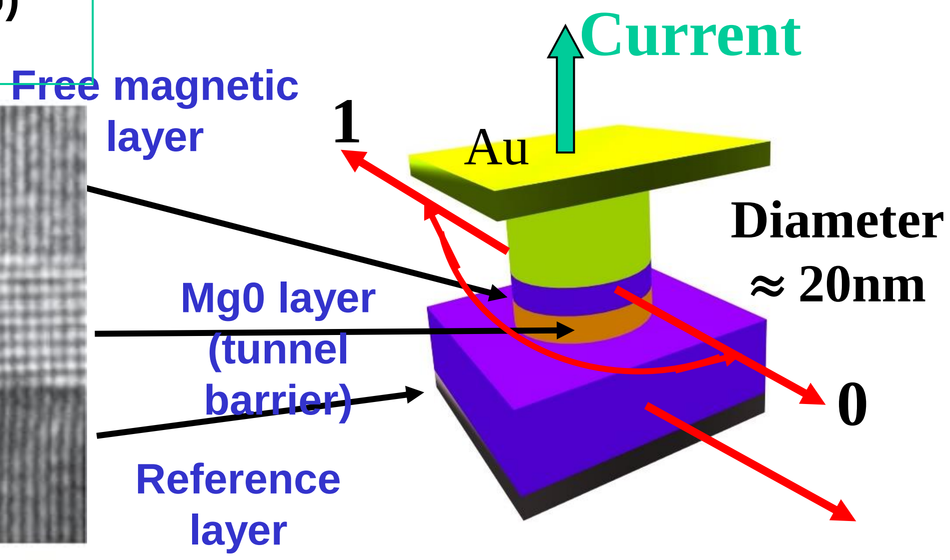
Electron tunneling through a tunnel barrier (insulating material)



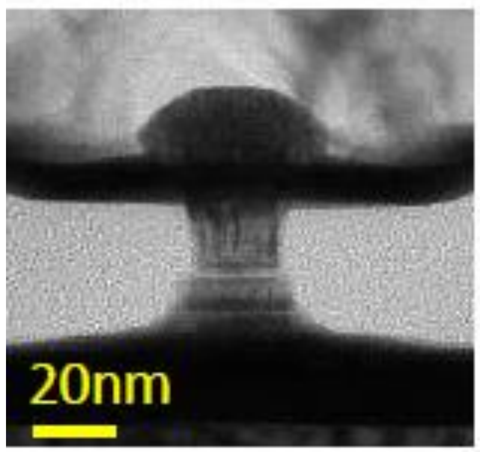
Magnetic Tunnel Junction (MTJ)
(ex: MgO between Fe, 2004)



Yuasa et al, Nat.Mat. 3, 868, 2004)



IBM (D.Worledge)



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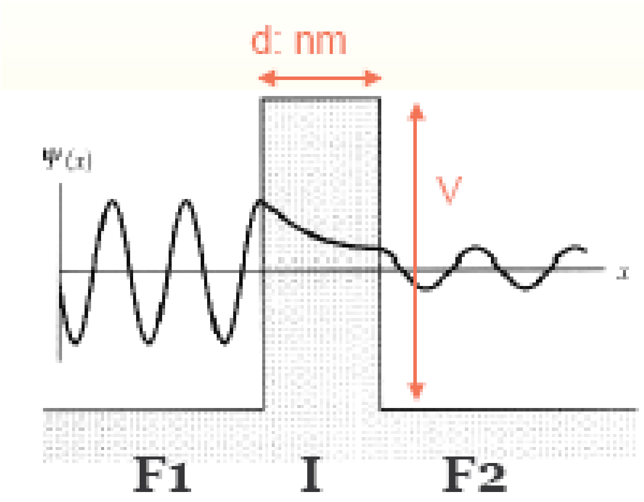

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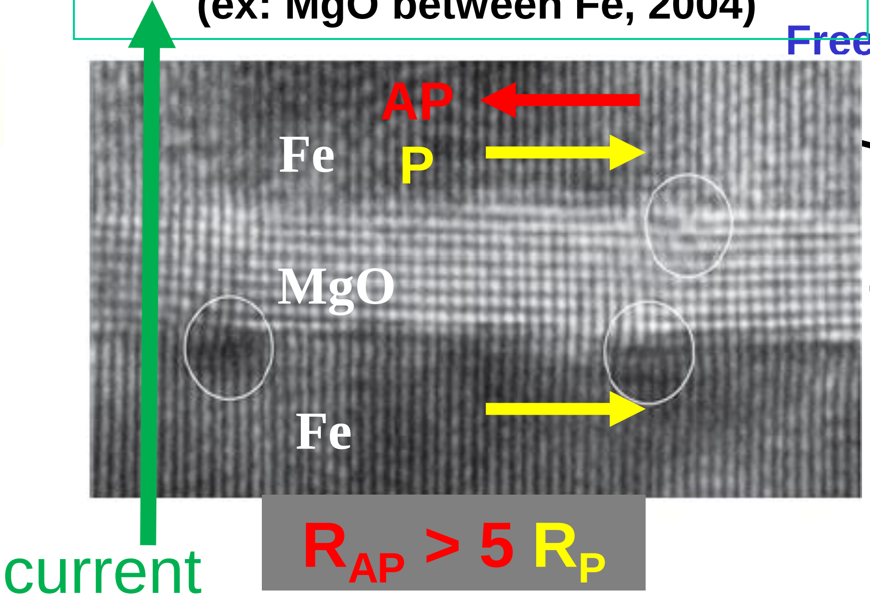

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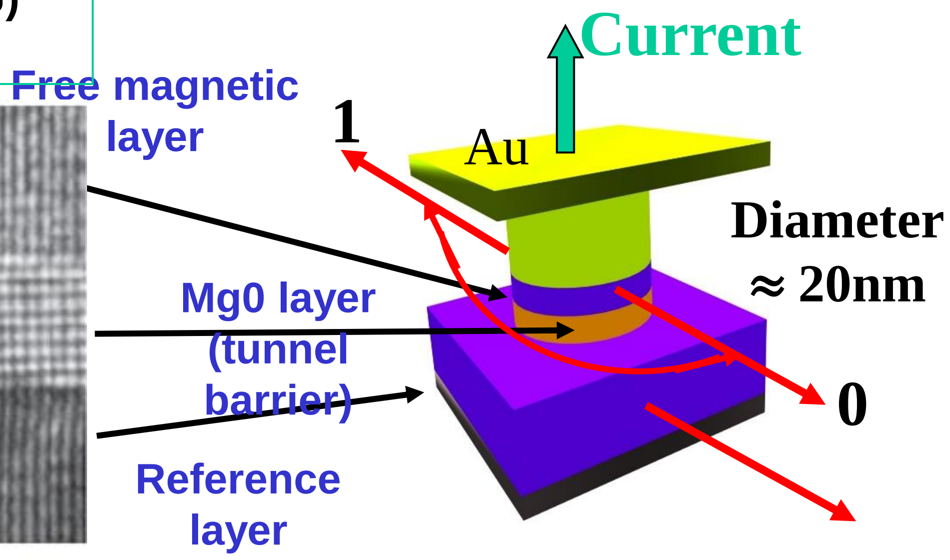

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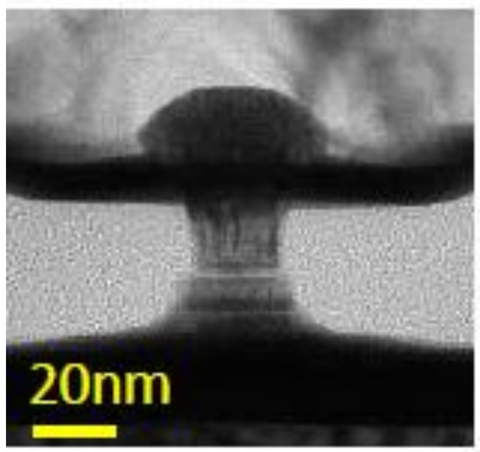

Reading by Tunnel Magnetoresistance ($R_{AP} > R_P$)

Writing by Spin Transfer Torque, important concept introduced by J. Slonczewski (JMMM 159, 1996) and L. Berger (Phys. Rev. B 54, 1996)

Magnetic Tunnel Junctions, Spin Transfer Torque (STT) and STT-RAM

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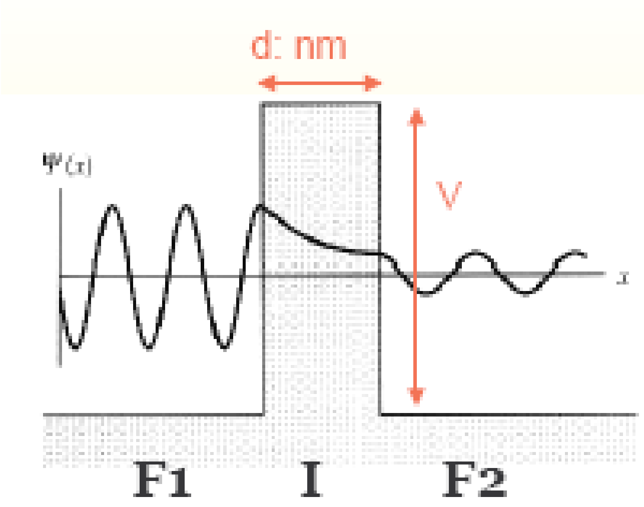

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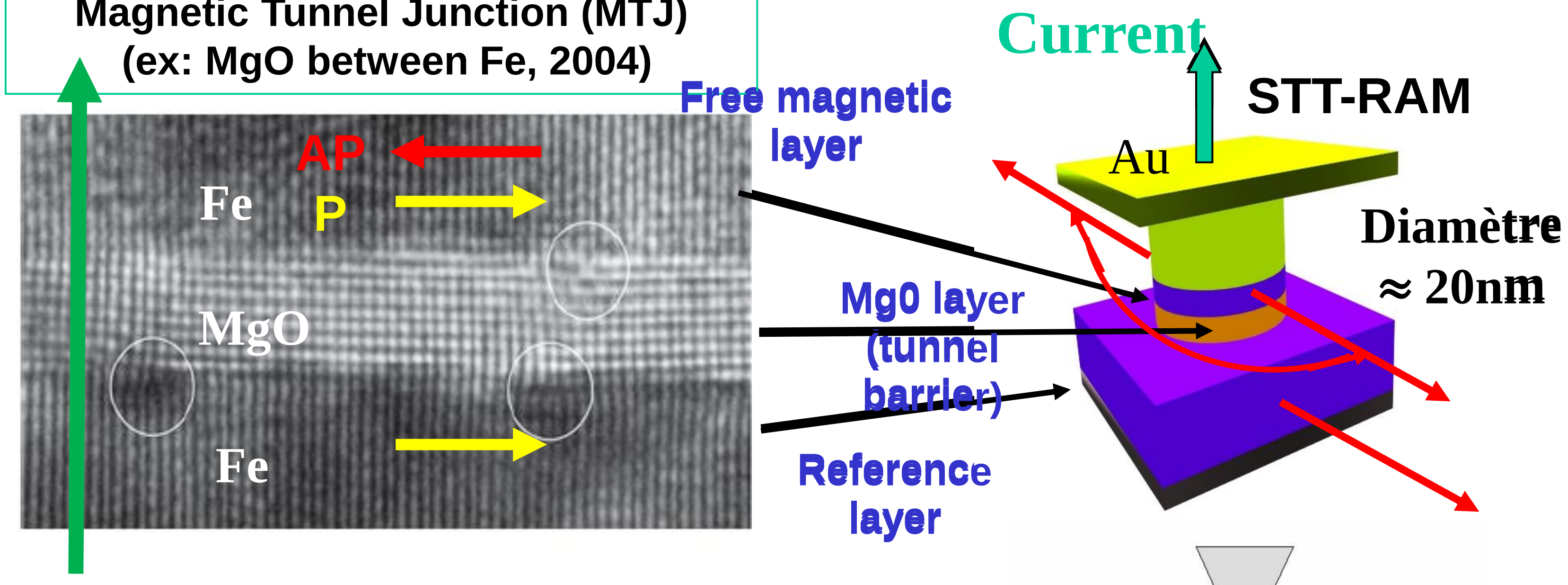
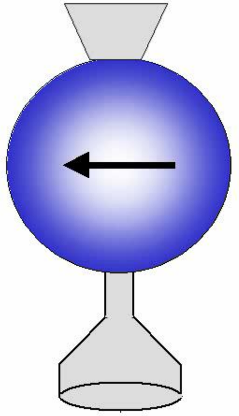
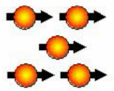


Writing by injection of magnetization from a spin-polarized curent and STT (spin transfer = transfer of magnetization)





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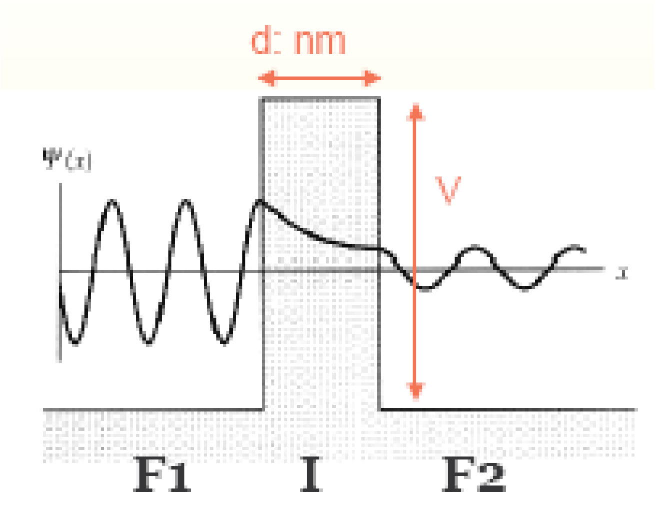

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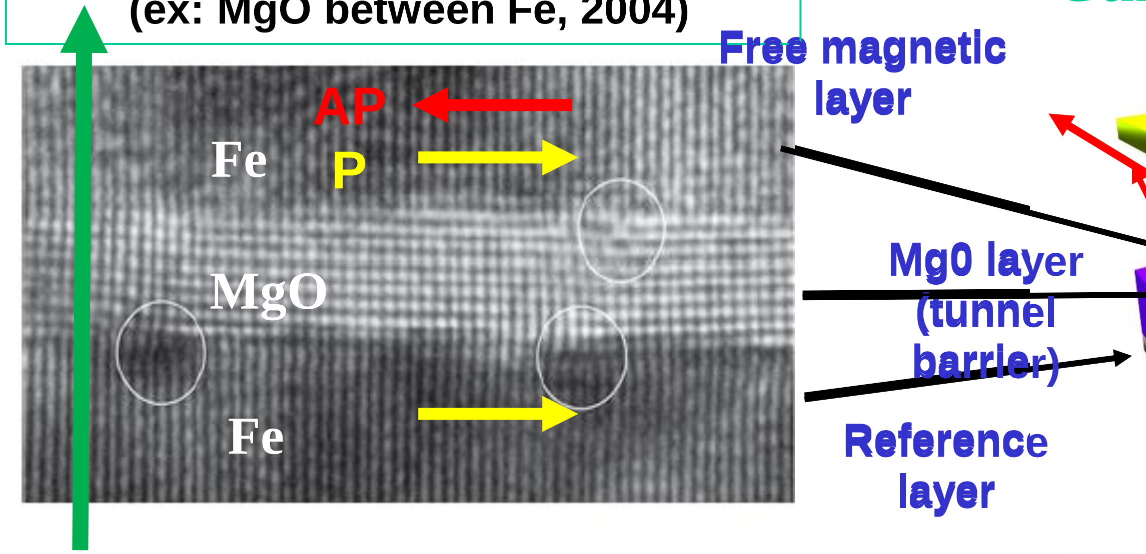

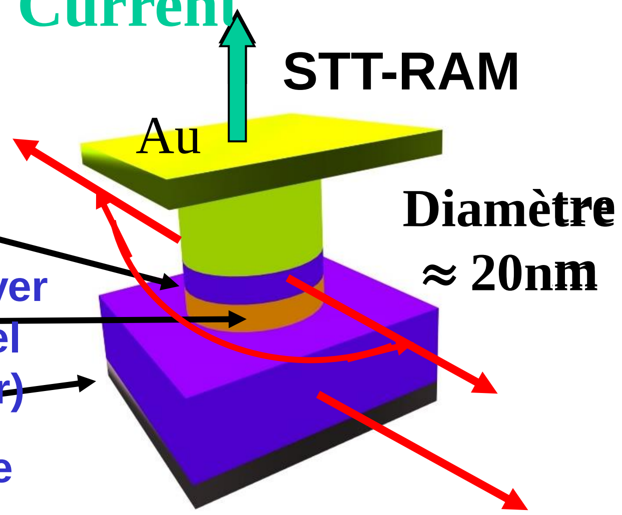

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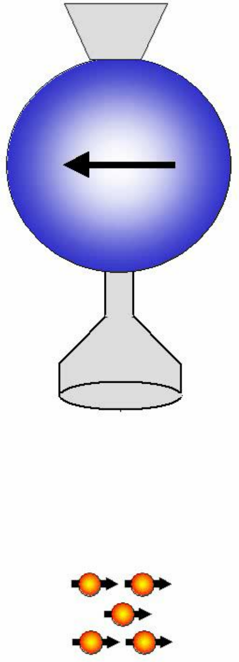
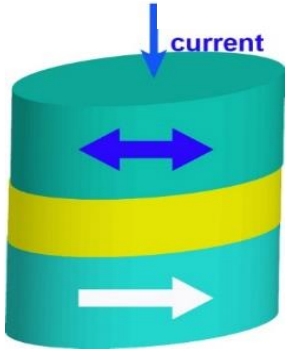


Main avantages of STT-MRAMs :
non-volatility + STT writing
→ low energy consumption

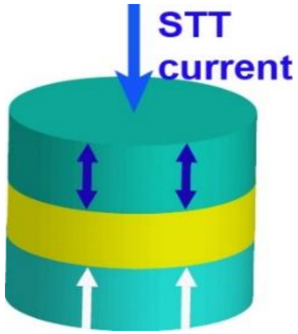
Magnetic Tunnel Junctions, Spin Transfer Torque and STT-RAM

MRAM



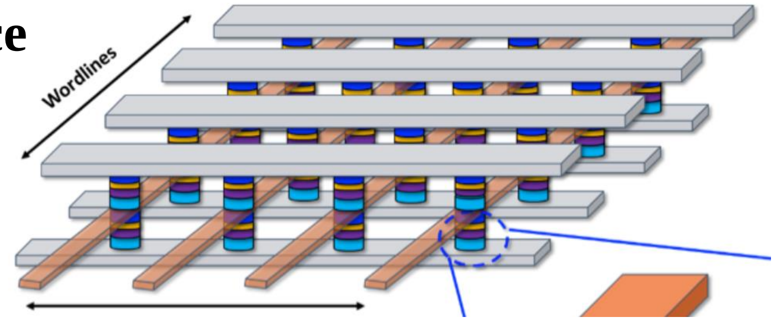
Since 2006 for avionic and aerospace

STT-MRAM



Since 2018

Array of STT-MRAMs



Europe: European Chip Act, 8/02/2022, Brussels.
(STT-RAM pilot-line at IMEC, Leuwen),
Global Foundries manufacturing plant atDresden
Intel: Project of foundrie in Magdeburg.
EU: Eur. Chip Act (2022), France: PEPR project

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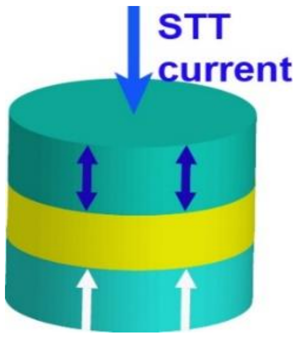
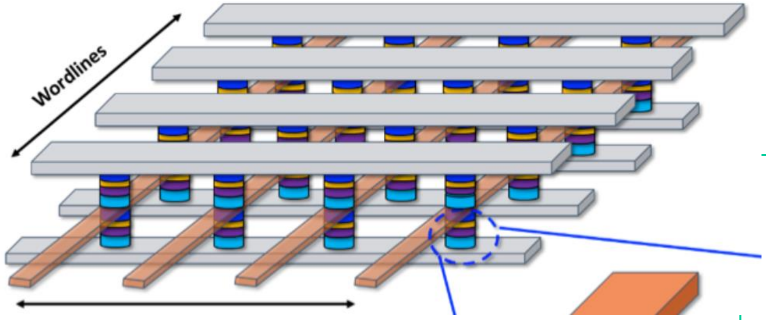
Next generation to go beyond STT-RAM: Spin-Orbit Torque (SOT) ans SOT-MRAM

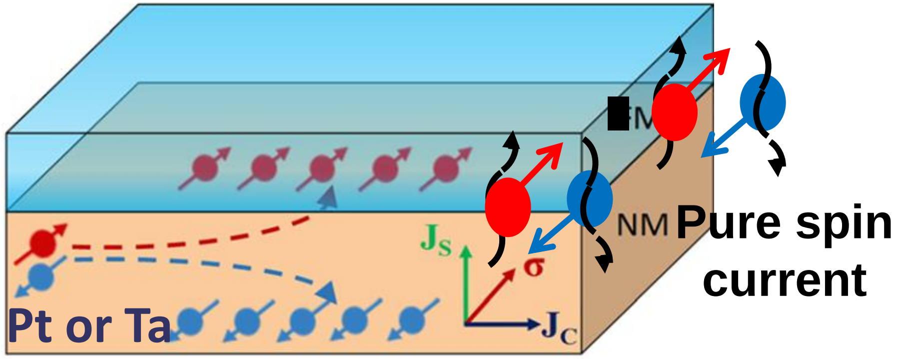
STT-MRAM



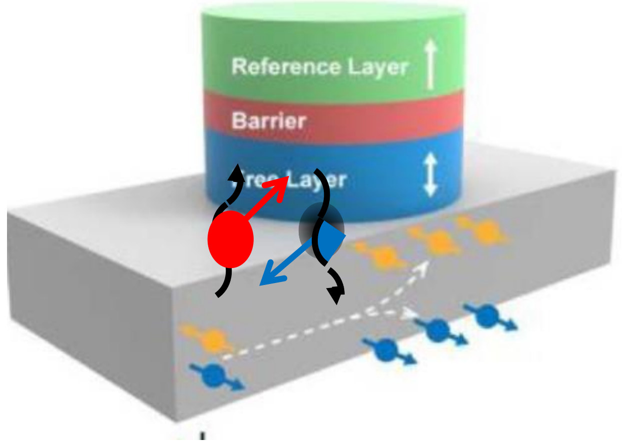


SOT-RAMs
(SOT= Spin-Orbit Torque)

Vertical spin current from SHE in Ta



Spin Hall effect



Main avantages
of STT-MRAMs or SOT-MRAMs:
non-volatility and low energy consumption + speed <ns for SOT

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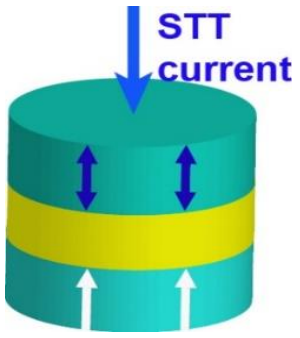
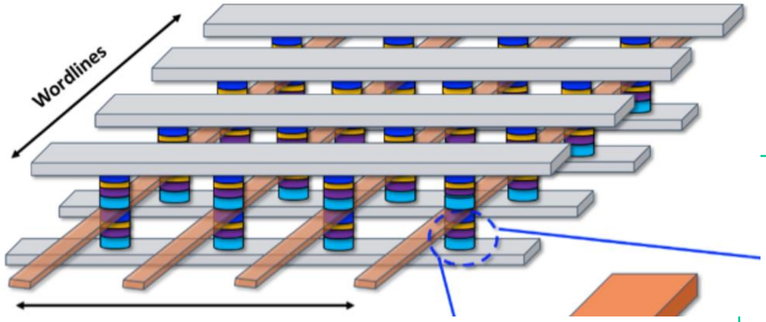
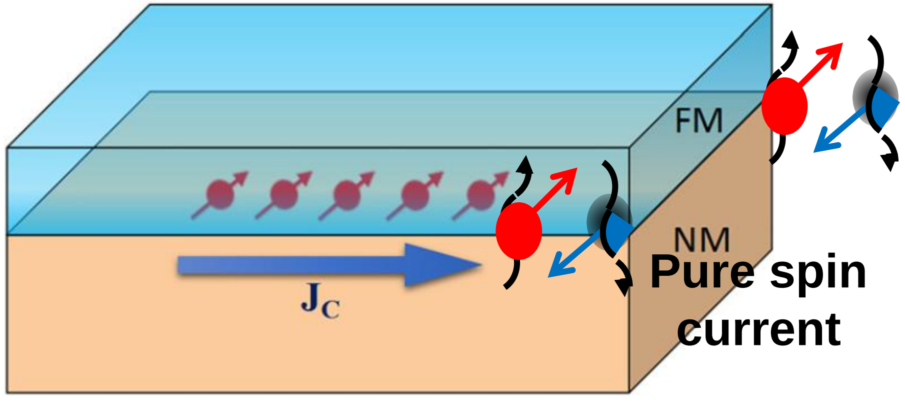
STT-MRAM



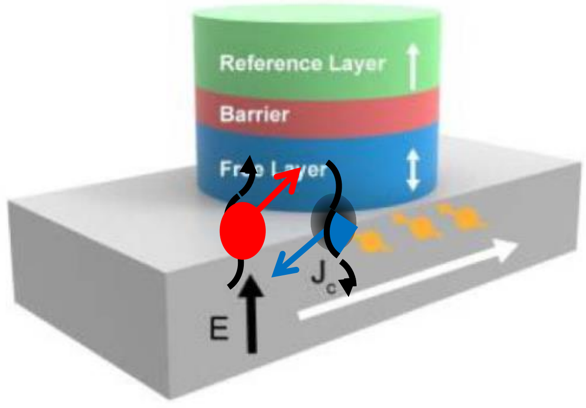


SOT-RAMs
(SOT= Spin-Orbit Torque)

Vertical spin current from Edelstein Effect in sruface states of topological insulator

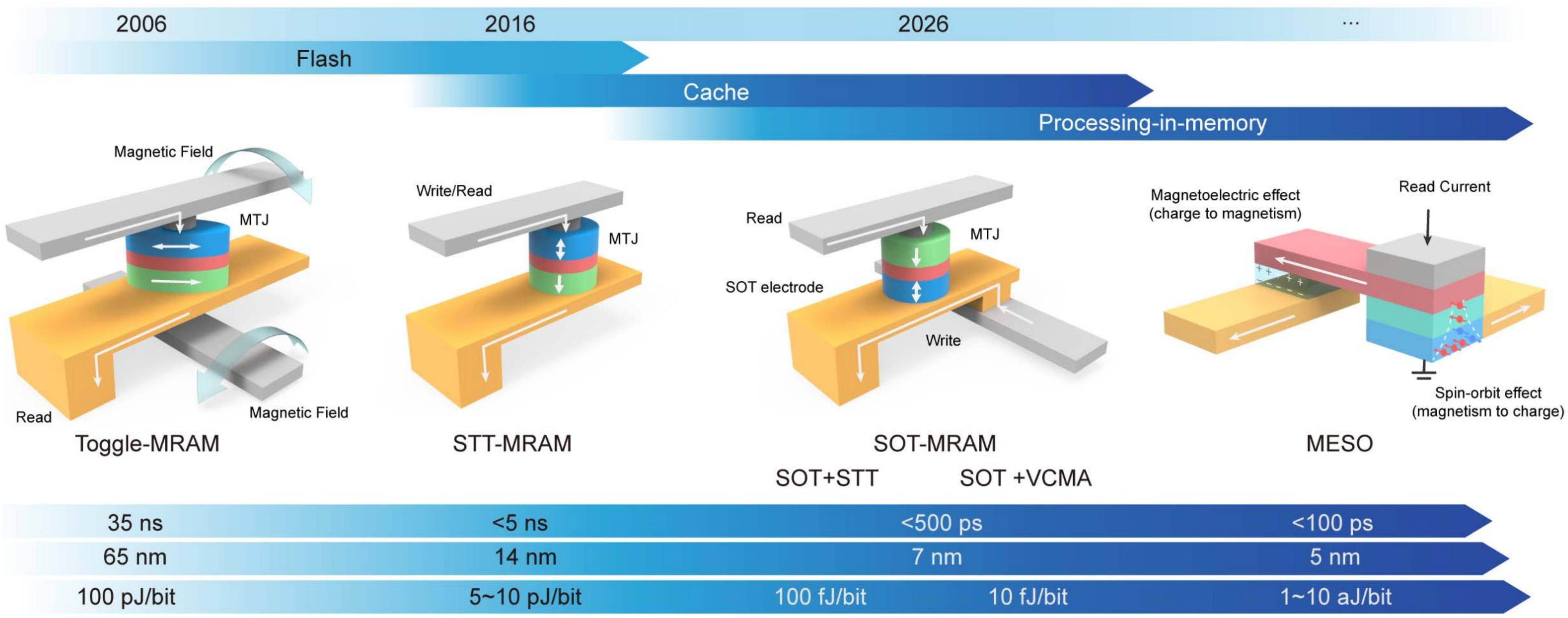


Rashba-Edelstein effect



Main avantages
of STT-MRAMs or SOT-MRAMs:
non-volatility and low energy consumption + speed <ns for SOT

a



2006
2016
2026
...
Flash
Cache
Processing-in-memory
Magnetic Field
MTJ
Read
Magnetic Field
Write/Read
MTJ
Read
MTJ
SOT electrode
Write
Magnetoelectric effect
(charge to magnetism)
Read Current
Spin-orbit effect
(magnetism to charge)
Toggle-MRAM
STT-MRAM
SOT-MRAM
MESO
SOT+STT
SOT +VCMA
35 ns
<5 ns
<500 ps
<100 ps
65 nm
14 nm
7 nm
5 nm
100 pJ/bit
5~10 pJ/bit
100 fJ/bit
10 fJ/bit
1~10 aJ/bit

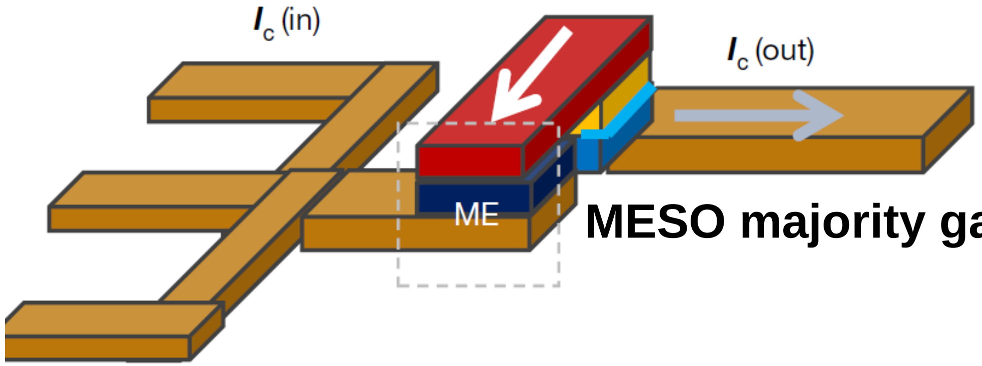
Feinman project between INTEL, UMR CNRS-Thales (PI: M. Bibes) and other laboratories for the development of MESO low power logic components

ME for Magneto-Electric, **SO** for Spin-Orbit

Scalable energy-efficient magnetoelectric spin-orbit logic

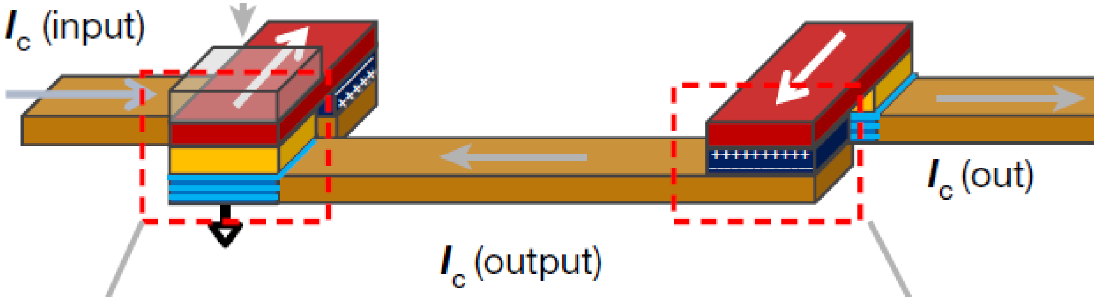
(**INTEL** publication, Manipatruni et al, Nature 565, 35, 2019)

We describe progress in magnetoelectric switching and spin–orbit detection of state, and show that in comparison with CMOS technology our device has superior switching energy (by a factor of 10 to 30), lower switching voltage (by a factor of 5) and enhanced logic density (by a factor of 5). In addition, its non-volatility enables ultralow standby power.



MESO majority gate

MESO interconnect with cascaded gates



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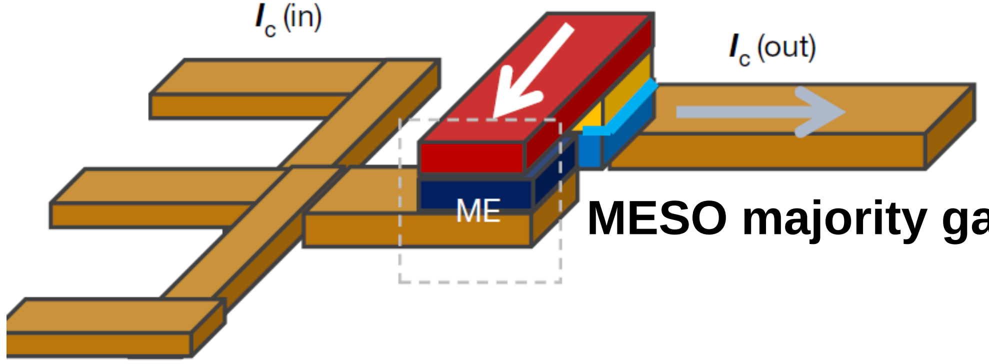

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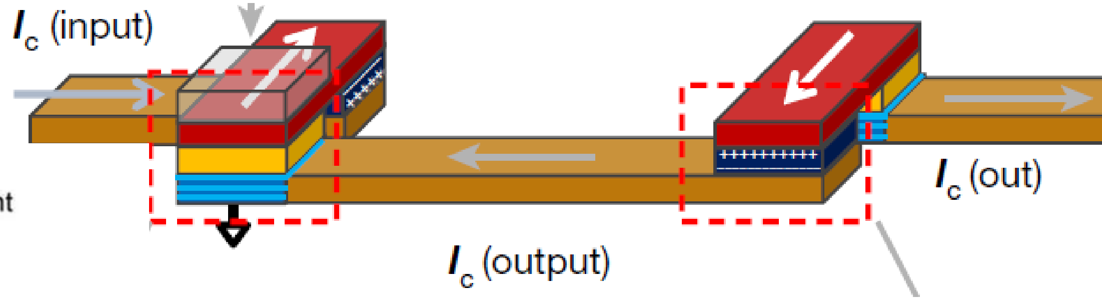

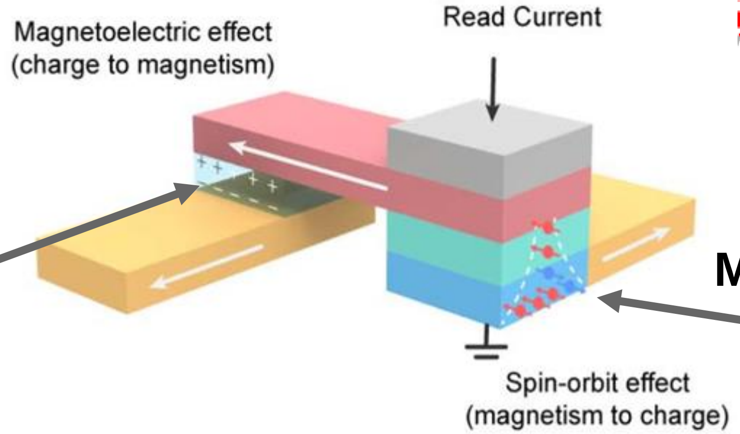

Control of FM magnetization by magnetoelectric coupling with input voltage (≈100 mV) through the ferroelectric polarization of a multiferroic

Magnetization to output voltage by spin to charge conversion via Spin-Orbit (inverse SHE or inverse Edelstein)

Multiferroics: Agnès Barthélémy,2021 IUPAP Magnetism Award. Spin-charge conversion with STO, Vaz, AF et al, Nat. Mat.2019

Intel annonce la création d'un centre de R&D et d'un centre de conception pour son service de fonderie en France

Publié par Frédéric Fassot | 15 Mar 2022 | - ECO -, - UNE -, ETATS-UNIS, EUROPE, FRANCE, SEMICONDUCTEUR, STRATÉGI

La France, reconnue pour sa puissance d'innovation, a en effet été choisie comme pays d'accueil du nouveau centre Européen de R&D, dont un premier site sera situé aux alentours du Plateau de Saclay dans le sud-ouest de l'Île-de-France

Scalable energy–efficient magnetoelectric spin–orbit logic

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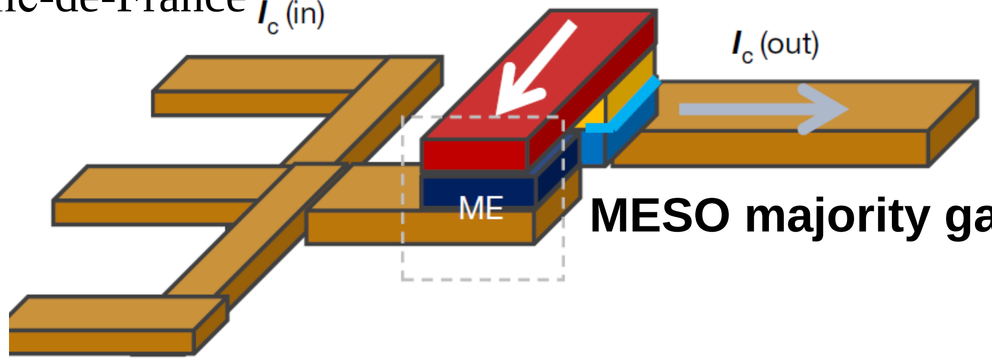

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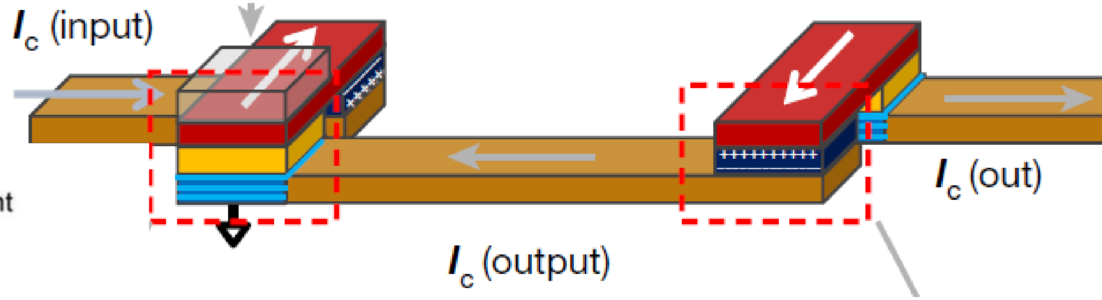

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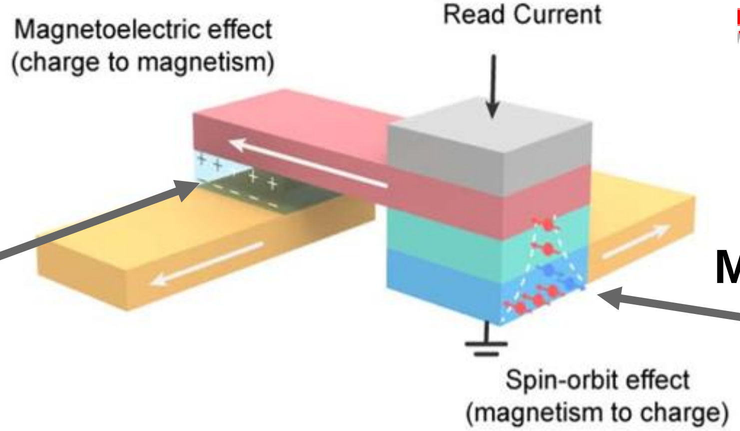

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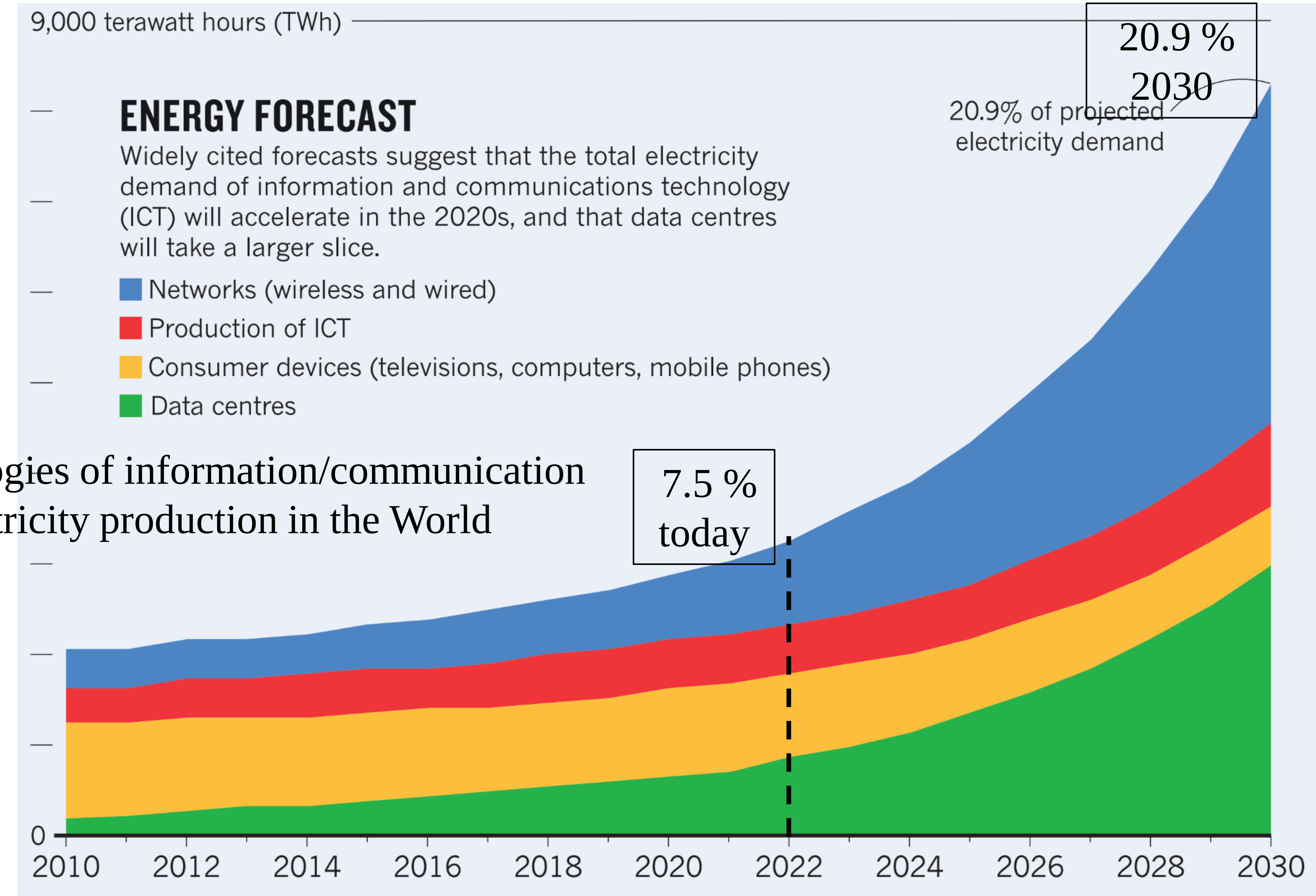
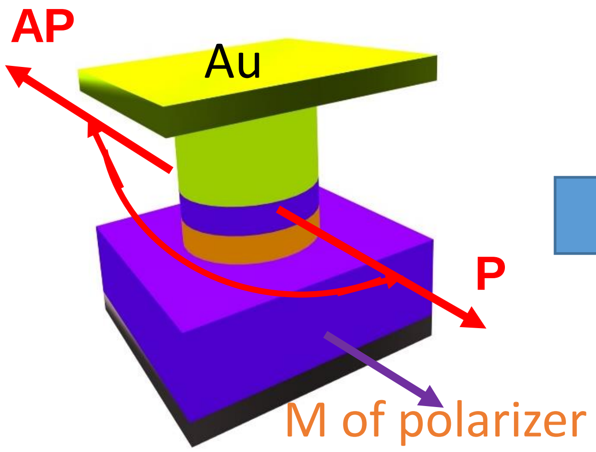
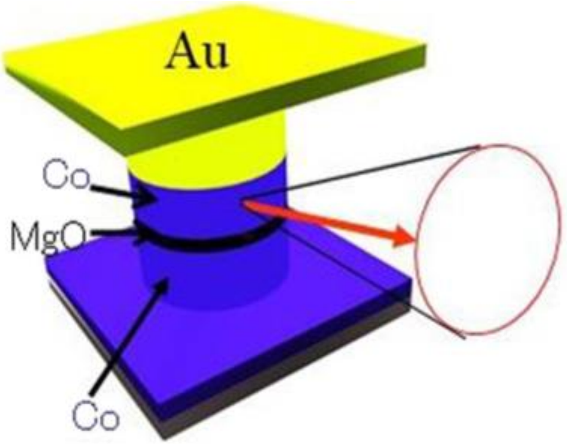


Demand of the technologies of information/communication in % of the electricity production in the World

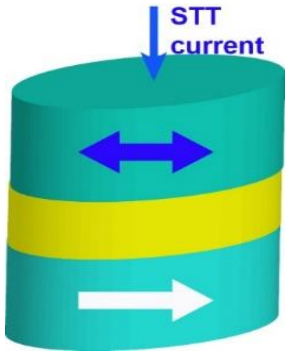
Andrea and Edler; Challenges, 6, 117 (2015) ; N. Jones, Nature 561, 163 (2018)

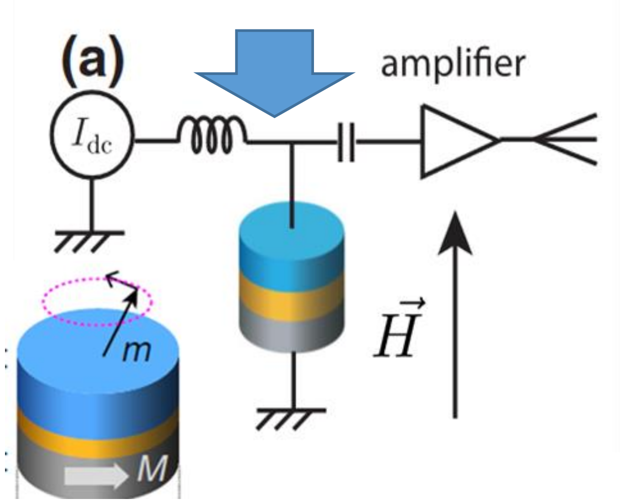
STT or SOT ⇨ other applications than STT-RAM: rf Spin Oscillators, Spin -Diode



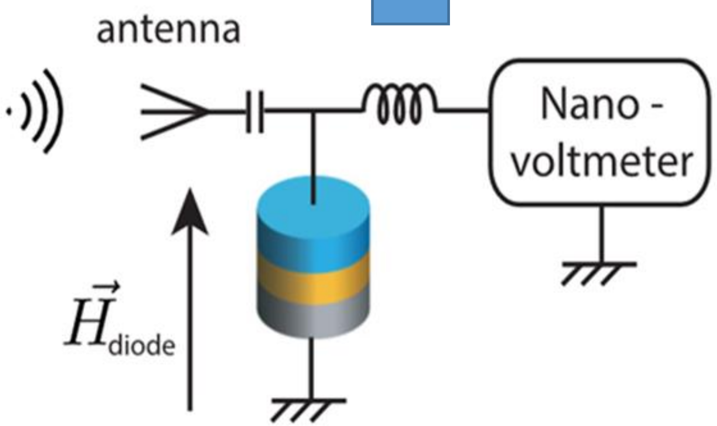


STT-MRAM





Spin Oscillator (STNO) for tunable rf emission



Spin Diode for conversion of rf signal into dc voltage

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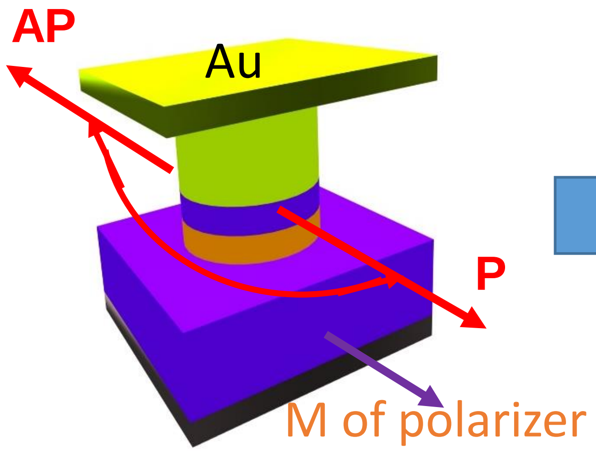
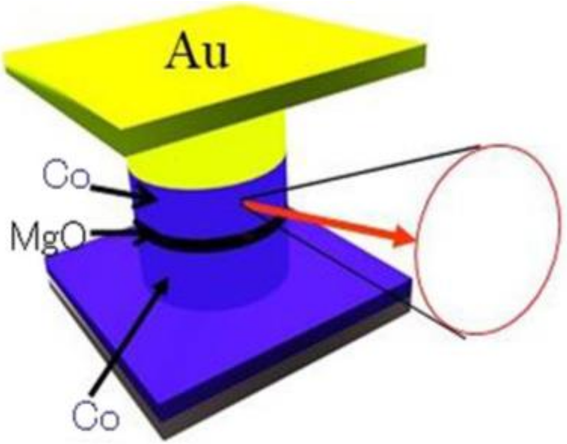
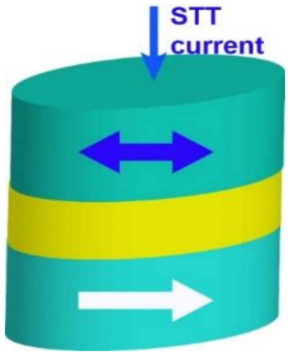
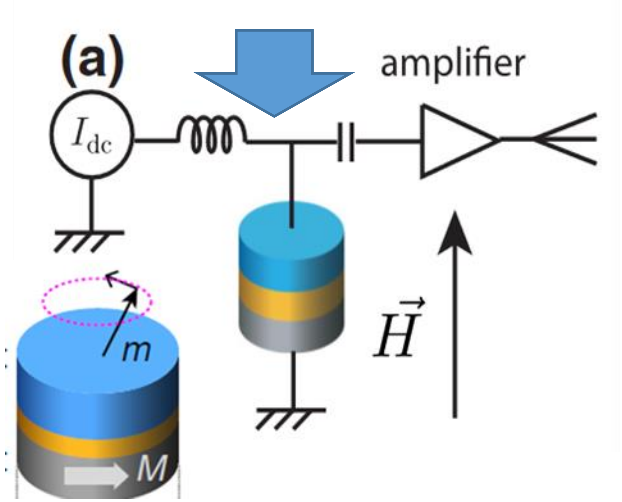




Harvesting ambient rf signals

STT-MRAM





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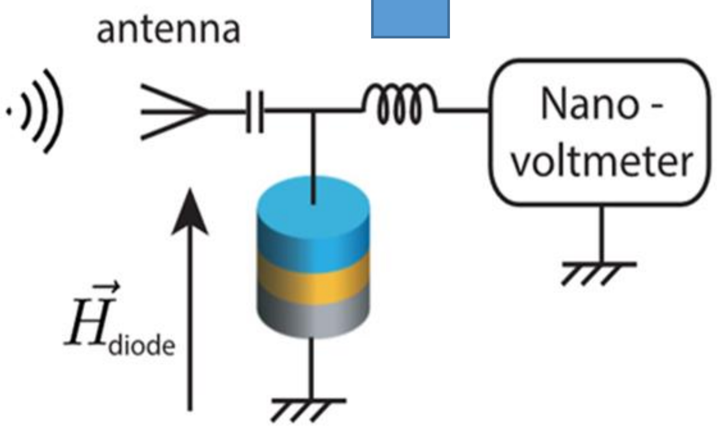

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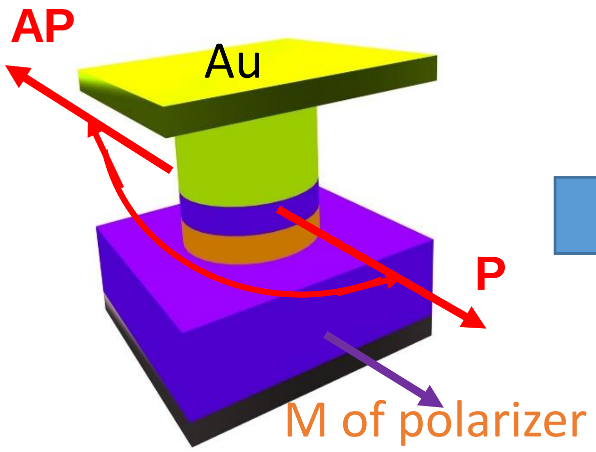
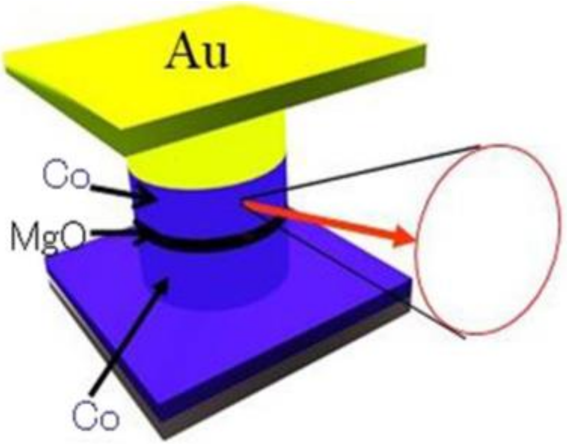
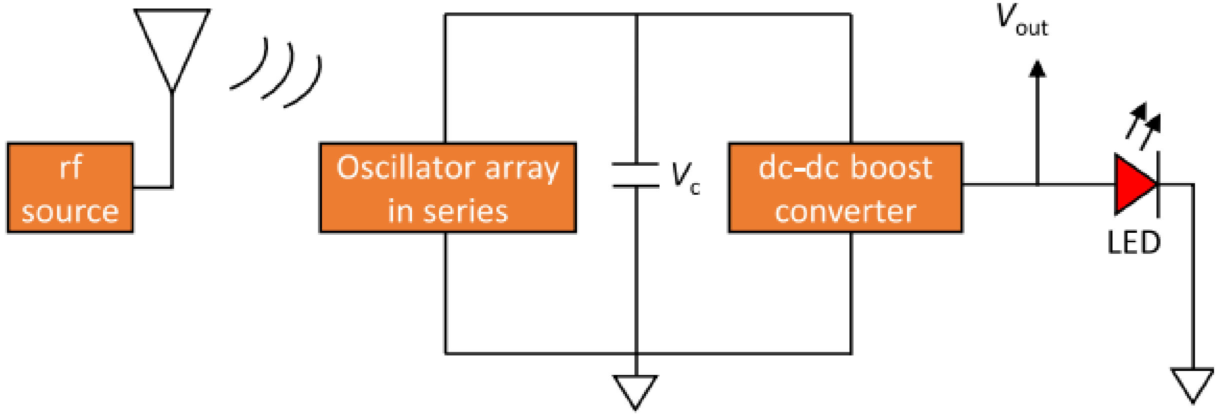
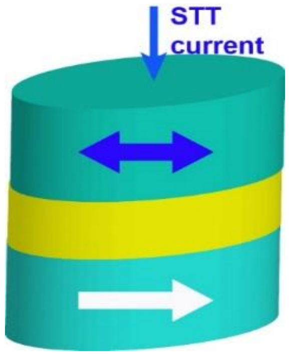


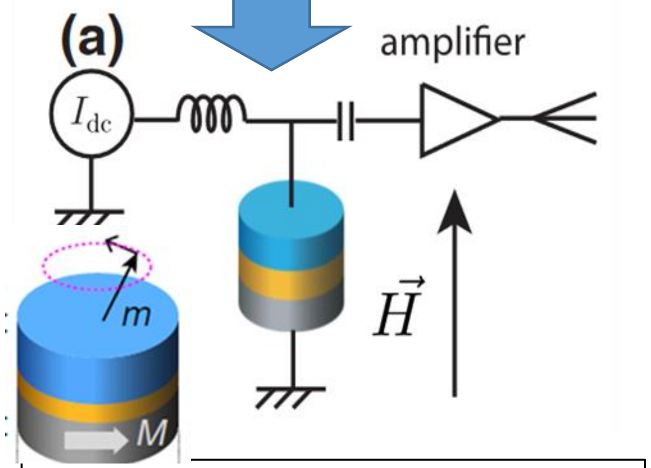


Harvesting of rf energy by spin diode

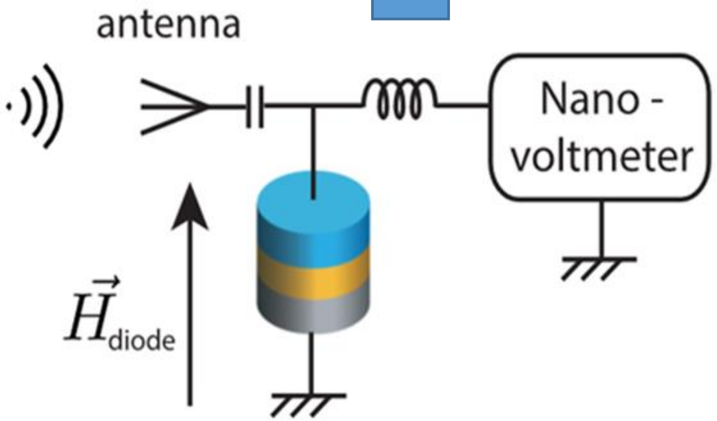


STT-MRAM





Spin Oscillator (STNO) for tunable rf emission



Spin Diode for conversion of rf signal into dc voltage

Spintronique: électronique sobre en énergie et plus encore (*spintronics to go beyond electronics and switch greener)*

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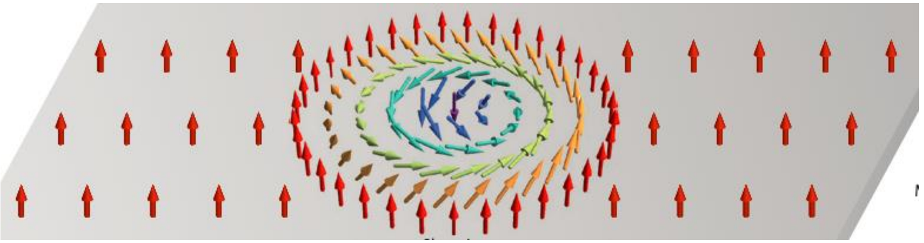
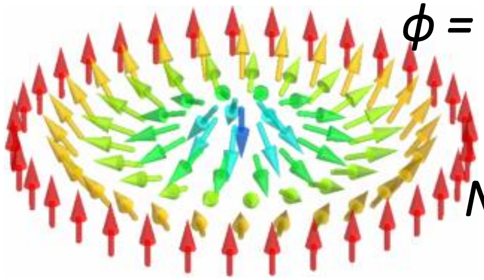
Review on skyrmions
AF, V. Cros and N. Reyren
Nature Review Mat. 2, 17031, 2017





Mathematical concept of topological protection has been introduced in 1962 by the British physicist Tony Skyrme in particle physics but magnetic skyrmions were observed for the first only in 2009 (Pfleiderer et al, University of Munich)

$$N_{Sk} = \frac{1}{4\pi}\int_{uc} dx\, dy\, \hat{m} \cdot (\partial_x \hat{m} \times \partial_y \hat{m}) = \pm 1 \ (topological\ number)$$

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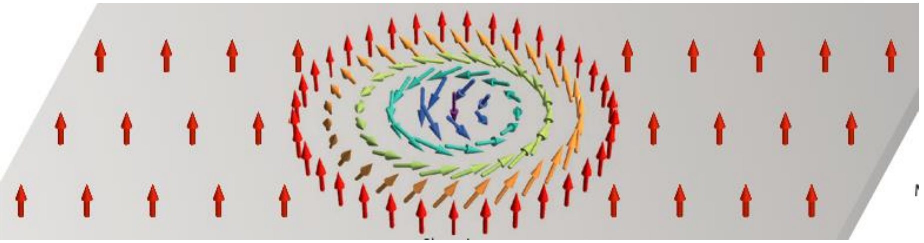
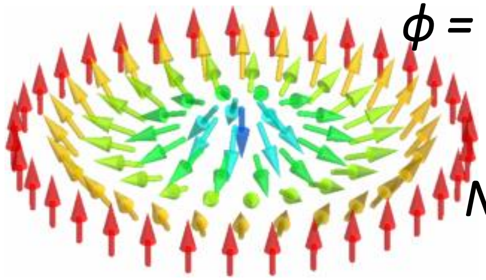


ϕ = 5-50 nm

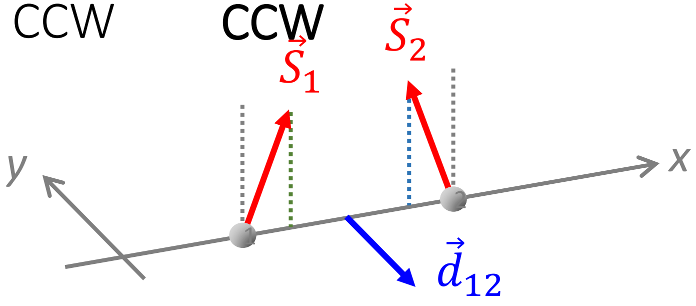


Néel skyrmion

CCW CCW

Mechanisms (in most systems): Dzyaloshinskii-Moriya Interactions(DMI)
(if SOC + no inversion symmetry)

$$H_{DMI} = -(\vec{S}_1 \times \vec{S}_2).\vec{d}_{12}$$



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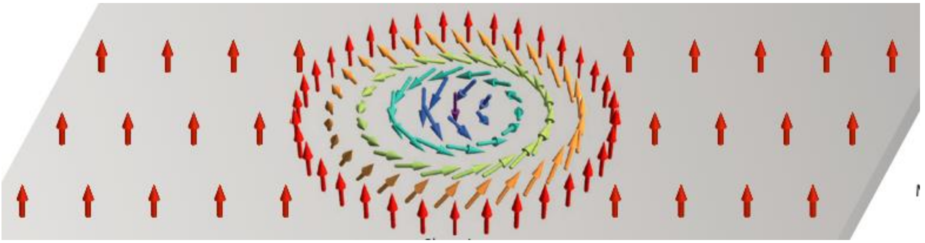

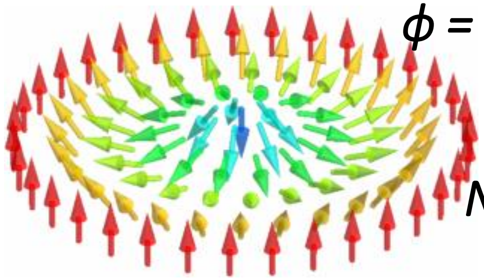

Mechanisms (in most systems): Dzyaloshinskii-Moriya Interactions(DMI)
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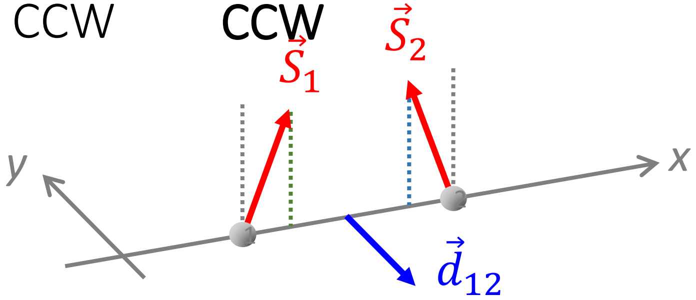
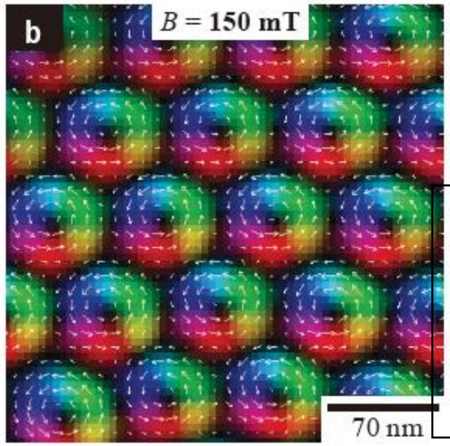
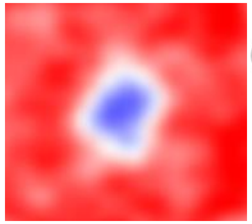
$$H_{DMI} = -(\vec{S}_1 \times \vec{S}_2) \cdot \vec{d}_{12}$$



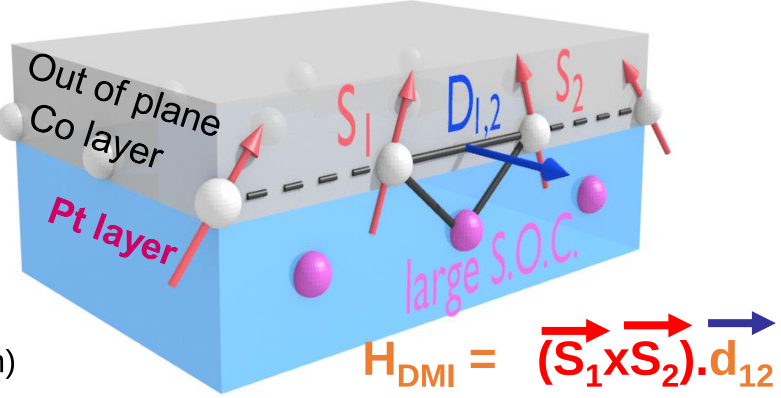


Yu et al, Nat.2010, skyrmion lattice in **noncentrosymmetric** material (Lorentz Mic.)

Co/Pt mml



MFM image
(diamètre: 80nm)



$$H_{DMI} = (\vec{S}_1 \times \vec{S}_2) \cdot \vec{d}_{12}$$

First introduced by **Dzyaloshinskii *(1957)*** and **Moriya *(1960)*** for non-centrosymmetric magnetic insulators with super-exchange.

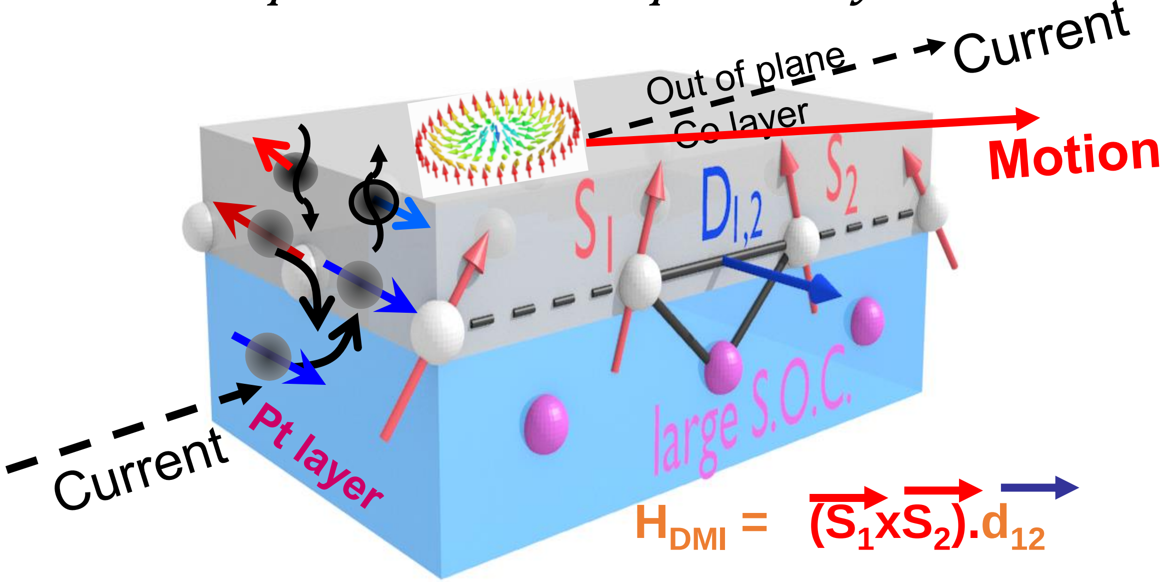
Extension DMI to metals (RKKY-like mechanism), first for disordered alloys (**AF and PM Levy**, PRL 44,1980) with extension to interfaces (**AF**, Mat.Sci. Forum 59-60, 1990)

Current-induced motion of skyrmions by SHE-induced pure spin current emitted by heavy metal + Spin Tranfer TorqueTT

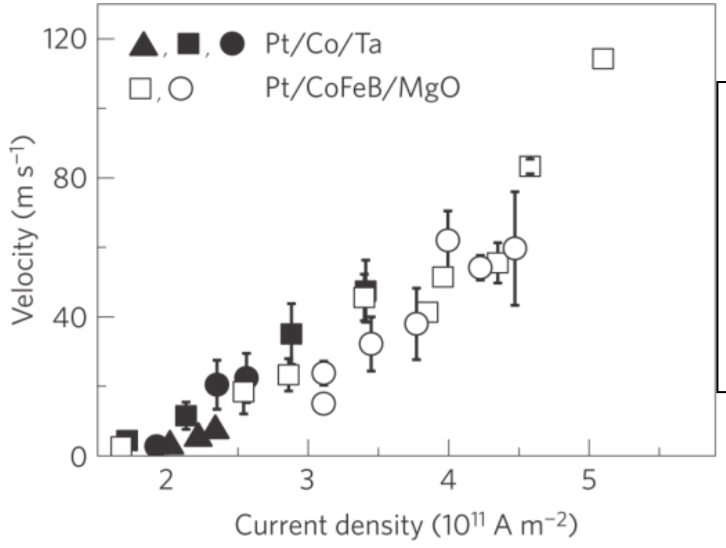
Spin Hall Effect (SHE): *opposite deflections of opposite spins*

→ *pure spin current injected into adjacent magnetic layer*

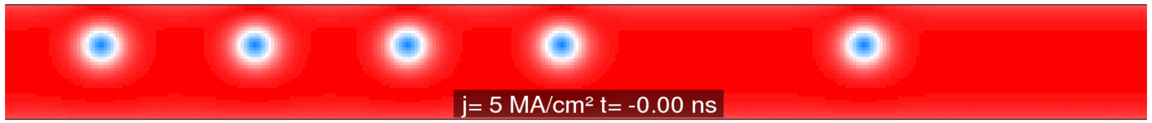
→ *Spin Transfer Torque on skyrmion and motion*

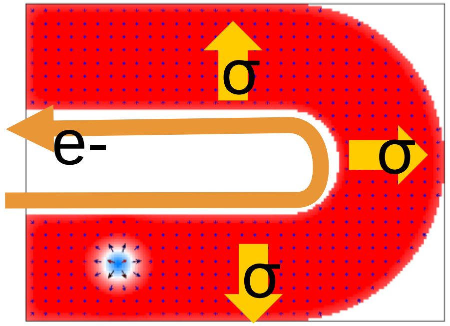


S. Woo et al,
Nat. Mat. 2015



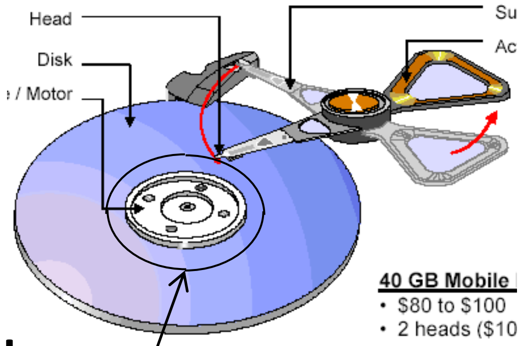
V = 100 m/s leads to 20 nm covered in 200 ps



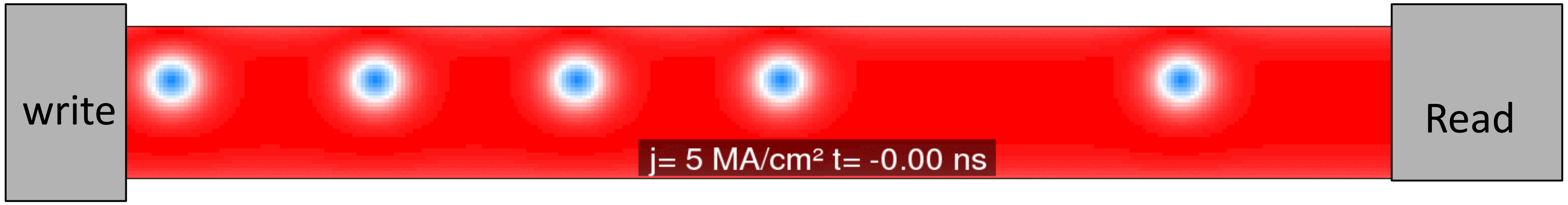


Skyrmions for information storage and processing?

Drawback of Hard Disk: mechanical system to move read/write head



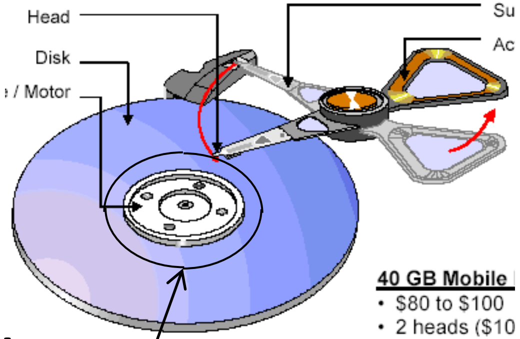
Concept of « Race track memory » with skyrmions: information is coded in a train of skyrmions which can be moved from writing head to read without mechanical system (low power)

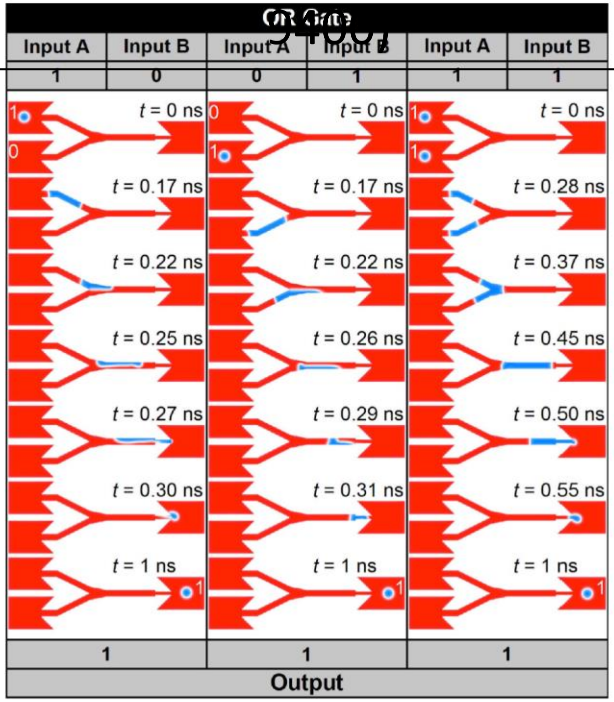


Skyrmions for information storage and processing?

Logic gate based on skyrmions (Zhang et al, Sci. Rep. 5,

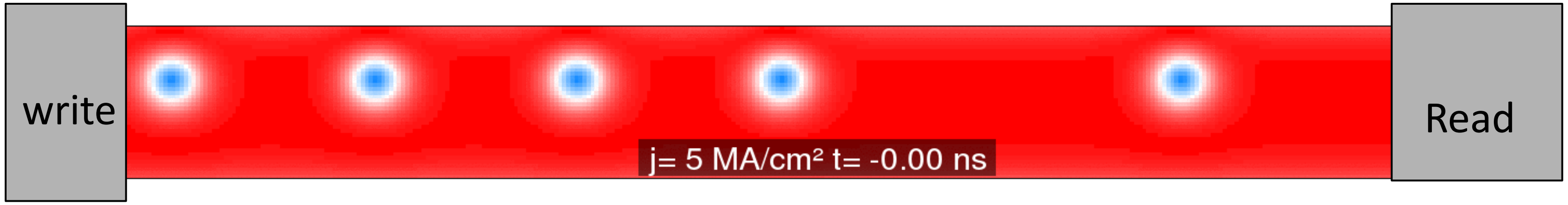
Drawback of Hard Disk: mechanical system to move read/write head





Exemple: OR gate based on the conversion between input skyrmions and domain walls .

Concept of « Race track memory » with skyrmions: information is coded in a train of skyrmions which can be moved from writing head to read without mechanical system (low power)

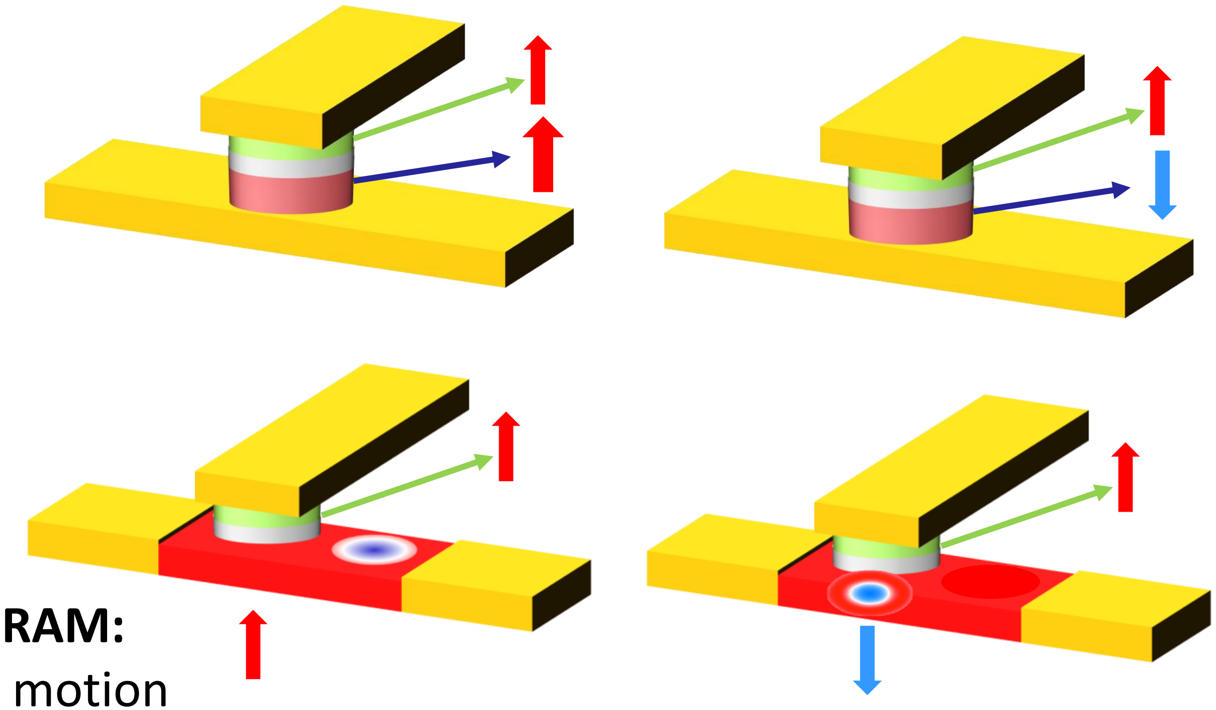


Skyrmion-MRAM

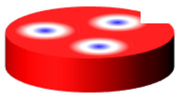
Skyrmion-mRAM

Memory state 0 **Memory state 1**

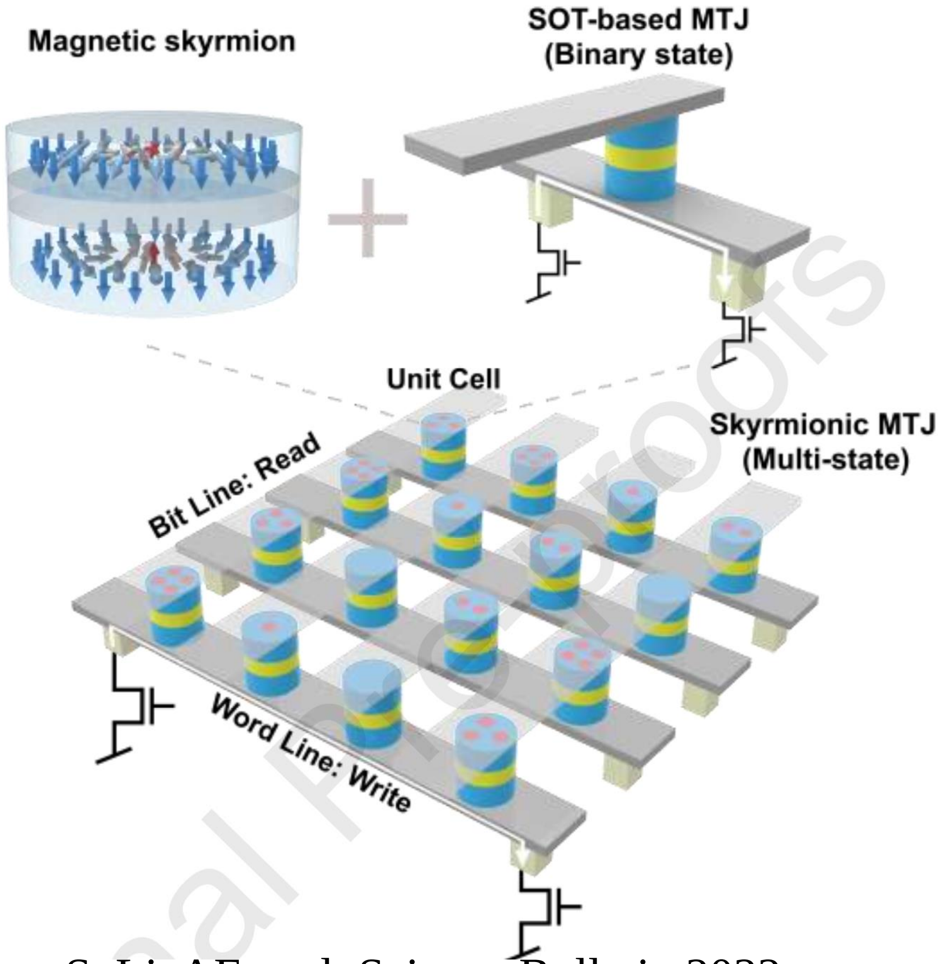
STT-RAM



Skyrmion-RAM: switching by motion of skyrmion under tunnel junction



Multistate memory with several skyrmions



S. Li, AF et al, Science Bulletin 2022
Experimental demonstration of skyrmionic magnetic tunnel junction

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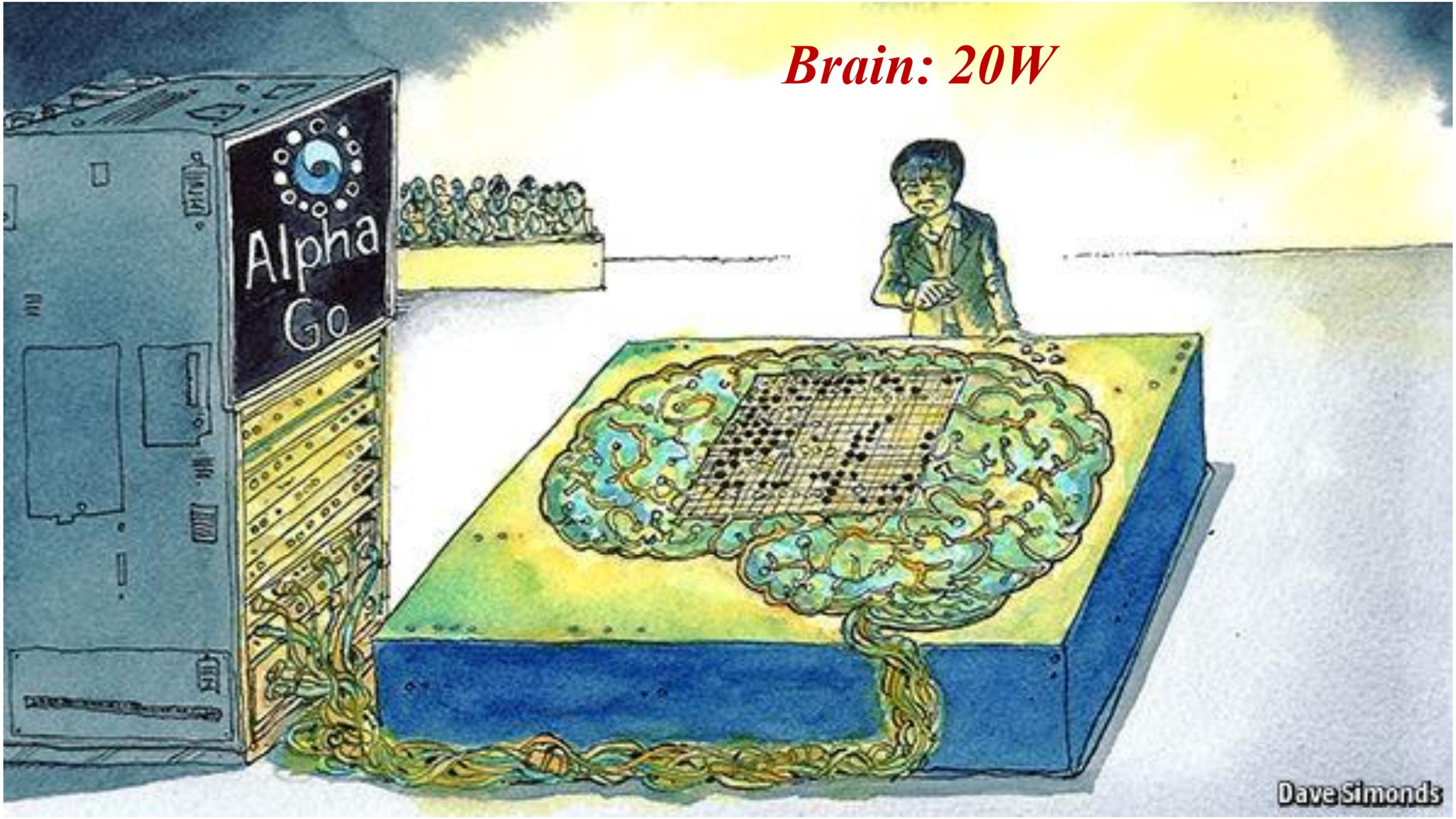
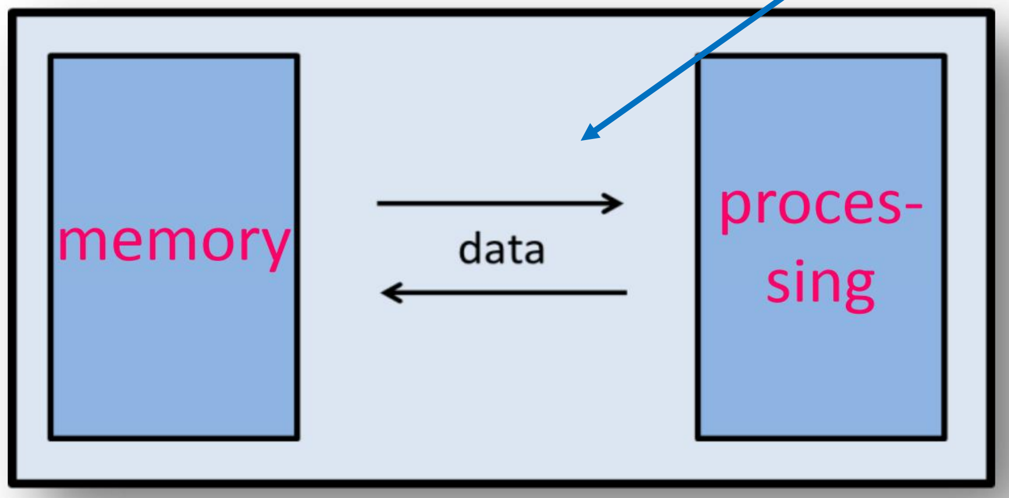
AlphaGo: 150 kW



Von Neumann’s bottleneck: separation between memory and processing:energy hungry back and forth data exchange, nonscalable for massive interconnections

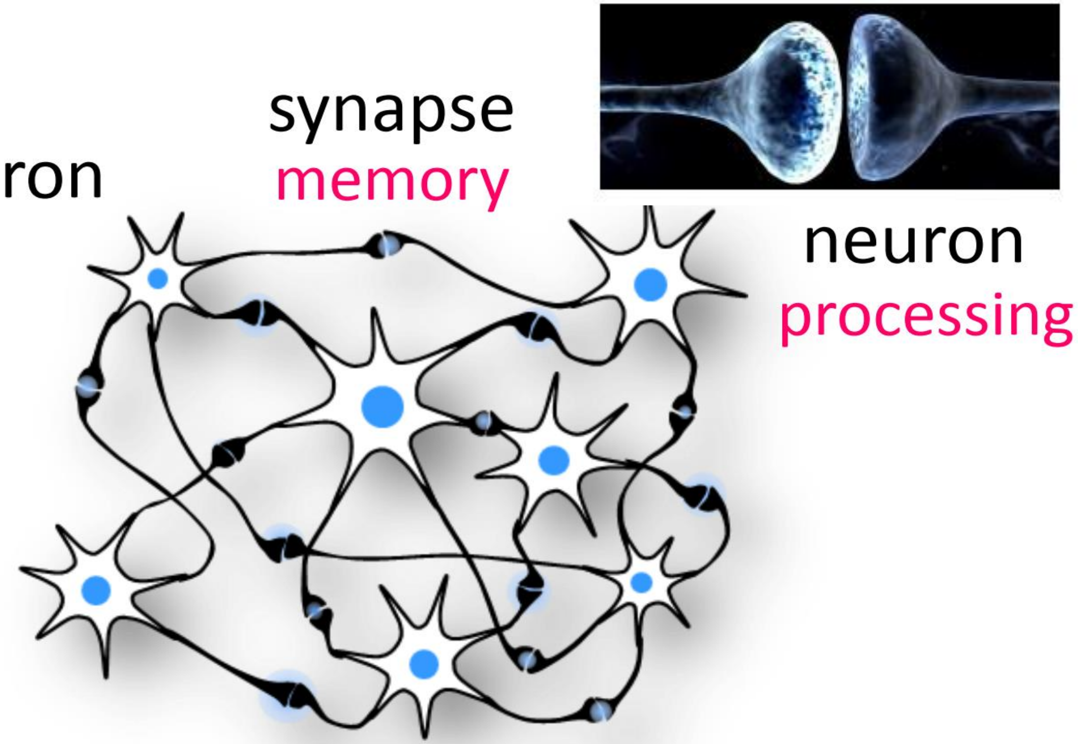
Digital computer



100 W/cm^2

Brain

Learning = tuning synapses



20 W in total !

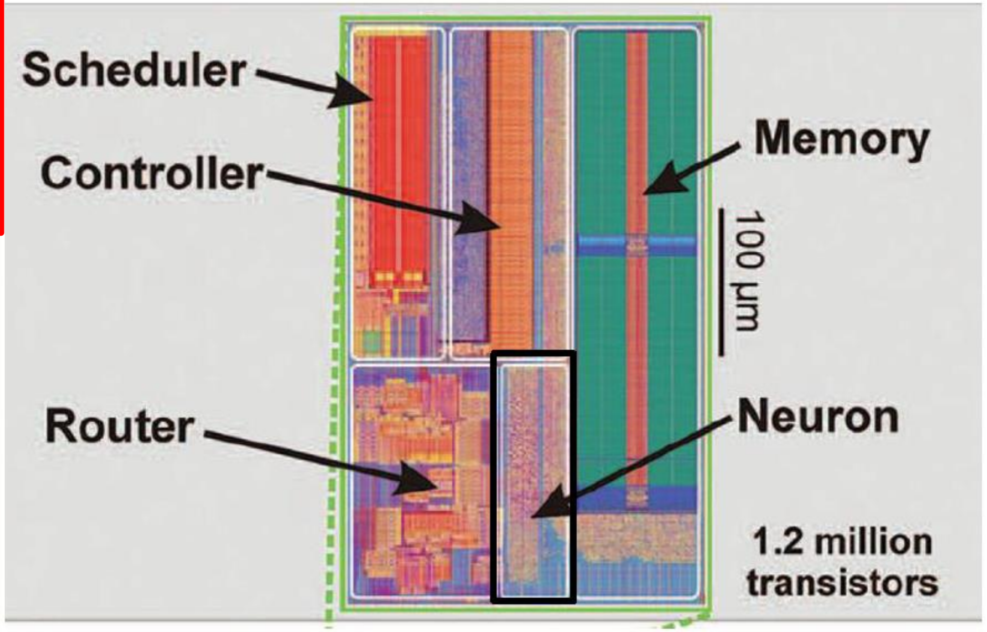
IBM's TrueNorth neuromorphic computer (artificial synapses + multiplexed artificial neurons)

Synapses: micro-circuits
with ≃ 50 – 100 transistors
size ≃ 10 μm

CMOS neuron **10-100 μm**

Brain :
10^{11}neurons,
10^{15} synapses
•Visual system:
500 millions of
neurons

Artificial neurons and synapses of today are big CMOS micro-circuits (> 10μm)



Merolla et al, *Science* **345**, 668 (2014)

CMOS technology leads to big sizes and large energy consumption

CMOS technology does not provide memory (separated processing and memory)

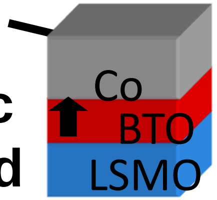
Future of neuromorphic computers:
nanoscale component acting individually as a neurone or a synapse

below, promising examples of ***nanoscale spintronic neurone and synapse***

Learning through ferroelectric domain dynamics in solid-state synapses

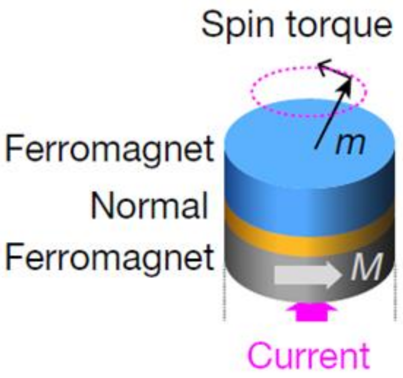
NATURE COMMUNICATIONS | 8:14736 |
DOI: 10.1038/ncomms14736

Tunnel junction with ferroelectric barrier in red



Neuromorphic computing with nanoscale spintronic oscillators

Jacob Torrejon[1], Mathieu Riou[1], Flavio Abreu Araujo[1], Sumito Tsunegi[2], Guru Khalsa[3]†, Damien Querlioz[4], Paolo Vincent Cros[1], Kay Yakushiji[2], Akio Fukushima[2], Hitoshi Kubota[2], Shinji Yuasa[2], Mark D. Stiles[3] & Julie Grollier[1]



42 8 | N A T U R E | V O L 5 4 7 | 2 7 J U L y 2 0 1 7

neuromorphic computers:
ng individually as a neurone or a synapse

f nanoscale spintronic neurone and synapse

Julie Grollier
Femme Scientique
de l'Année 2021

roelectric domain dynamics
ses

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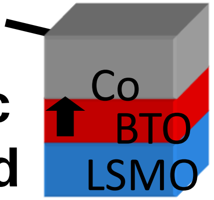

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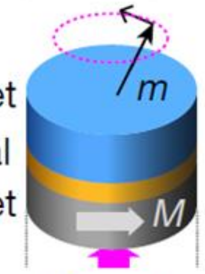

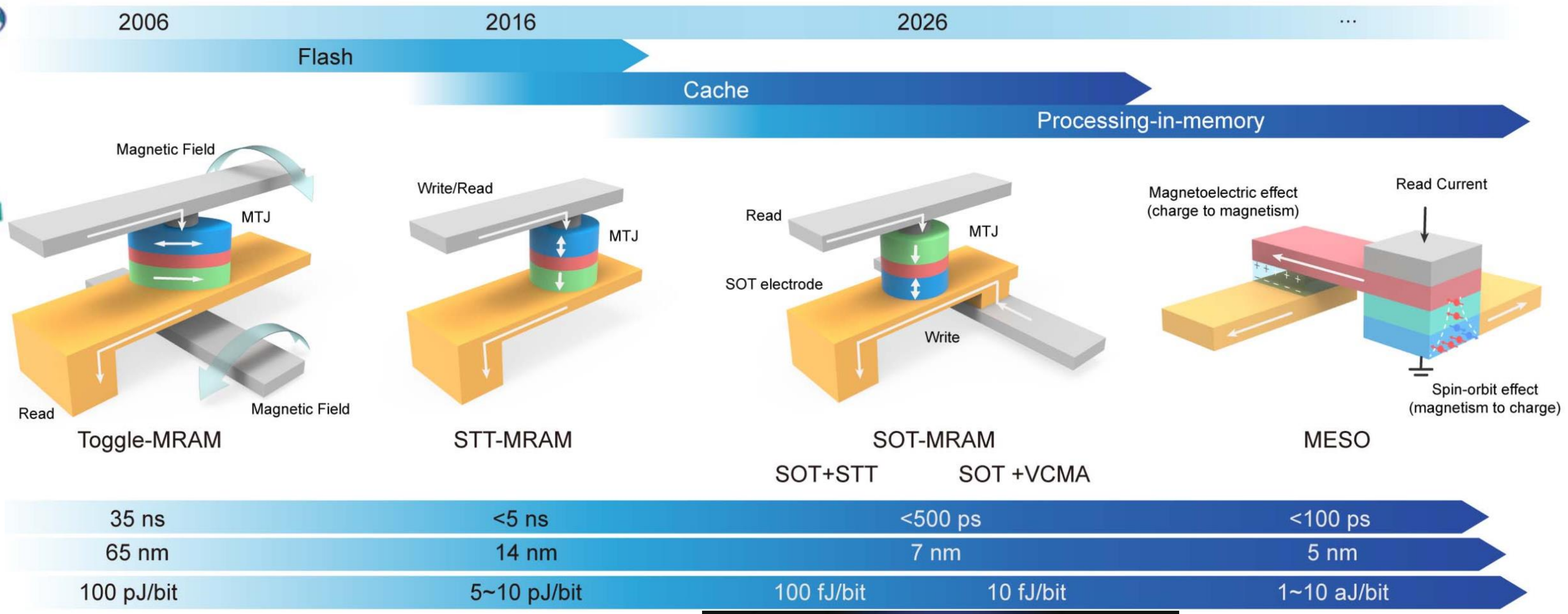

Conclusion: la spintronique devrait aider l’électronique à encaisser le choc énergétique du à l’explosion des transferts de données par les TICs. Cependant, pour l’énorme industrie électronique, le changement ne peut être que progressif, vers 10% du marché de l’électronique prévu pour 2025.